Ph.D. DISSERTATION

Effective Solution-processed Deposition Techniques of Semiconducting Single-walled Carbon Nanotube for Next-generation Thin-Film Transistor

차세대 박막 트랜지스터를 위한 효율적인 용액공정기반 반도성 단일벽 탄소나노튜브의 박막 형성 방법들에 관한 연구

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DEPARTMENT OF ELECTRICAL AND
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COLLEGE OF ENGINEERING
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Abstract

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As the demand for flexible and stretchable electronic devices increases, underpinning technologies of system implementation based on the solution-process have been tremendously developed. In particular, solution-processed random networks of semiconducting single-walled carbon nanotubes (SWCNTs) have been widely studied as suitable semiconducting materials for thin-film transistors (TFTs) in next-generation novel applications such as large-area active matrix for lighting emitting devices or biosensors due to their superior electrical and mechanical properties. Furthermore, low-cost and low-temperature processability of highly purified semiconducting SWCNTs with dispersed ink facilitates realizing large-

area flexible and stretchable electronic systems. Among various deposition methods of SWCNT based on the solution-process, the easiest and the most effective method to fabricate the SWCNT TFT is directly dipping the substrate into the SWCNT ink, resulting in highly-feasible and highly-uniform deposition of SWCNT onto the large-area substrate, which is called “direct dipping method”. However, there are limitations to utilize it for the mass-production and commercialization at the related industry. First, this method exhibits low fabrication throughput due to a very long deposition time of SWCNT. And moreover, additional patterning process is needed because the substrate is wholly immersed into the SWCNT solution during dipping process. Therefore, to overcome these issues, some engineering modifications of strategy should be developed.

In this Ph. D. dissertation, I developed two facile and effective fundamental technologies, which are “multi-dipping technique” and “self-patterning technique (inkjet-printing of PLL technique)”, to resolve the aforementioned issues of direct dipping method. Multi-dipping technique is repeatedly both soaking a substrate into SWCNT solution with a very short time and rinsing the substrate each time for dramatically significant reduction of total deposition time of SWCNTs networks instead of soaking the substrate into the solution with a very long time. Compared to the conventional dipping method, this technique reduced the overall process time by more than half and improved the electrical characteristics of SWCNT TFTs at the same time. In addition, in order to achieve simultaneous patterning of the SWCNT layer during the direct dipping process, I inkjet-printed the surface functionalization material, especially the poly-L-lysine (PLL) material, enhancing the attachment of the semiconducting SWCNT

at the region where we want to attach the SWCNTs. Only on top of PLL-patterned region, the networks of semiconducting SWCNTs were formed during dipping process although the substrate was wholly immersed into the SWCNT solution.

Then, I combined the newly-desired two techniques for effectively fabricating the SWCNT TFT based on the direct dipping method and investigated the feasibility and applicability of the combined technology for the implementation of high-throughput and high-resolution SWCNT TFTs. I defined it as “fast and self-patterning technique”. In this dissertation, verification was conducted based on two criteria which are large-area scalability and micro-patternability, and for the verification of the latter one, I utilized electrohydrodynamic (EHD)-based printing technology that enables effective fabrication of fine pattern.

The two primary purposes of this dissertation are to develop the technologies for effective deposition of *in-situ* patterned high-quality SWCNT film at the desired area onto the large-area substrate and to investigate the feasibility of the integrated technique for the implementation of future electronic applications. Furthermore, low-temperature processability and excellent mechanical flexibility of SWCNT networks could provide a guideline for implementing roll-to-roll (R2R) fabrication of high-throughput, high-resolution, and high-performance SWCNT TFT array, which is ultimately for the commercialization of future advanced flexible/stretchable electronic applications.

Keyword : Solution-process; Semiconducting SWCNT; Multi-dipping; Inkjet-printing of PLL; Large-area scalability; Micro-patternability;

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Chapter 1

Introduction

1.1. Solution-processed Thin-film Transistors

Recently, flexible and stretchable electronics have received great attentions from many research groups and industries as the need for much higher user experience and interface of electronic devices increases. So, there are many applications and innovations related with these next-generation flexible/stretchable electronics such as stretchable display, hybrid electronic circuits, soft robotics, and wearable sensors [1-4] (Figure 1.1). Especially, to utilize and commercialize these applications, thin-film transistor (TFT) is one of the most important technologies because it could easily control the output signal of single pixel like light emitting device (LED) or sensor for operation of overall system with a form of active matrix. Furthermore, it could also provide minimized crosstalk of signal, which consequently enables the systems to exhibit better spatial resolution and fast response time [5-7].

Generally, to fabricate TFTs, there are two types of deposition method to deposit the each thin-film constituting the TFT, which are vacuum-process and

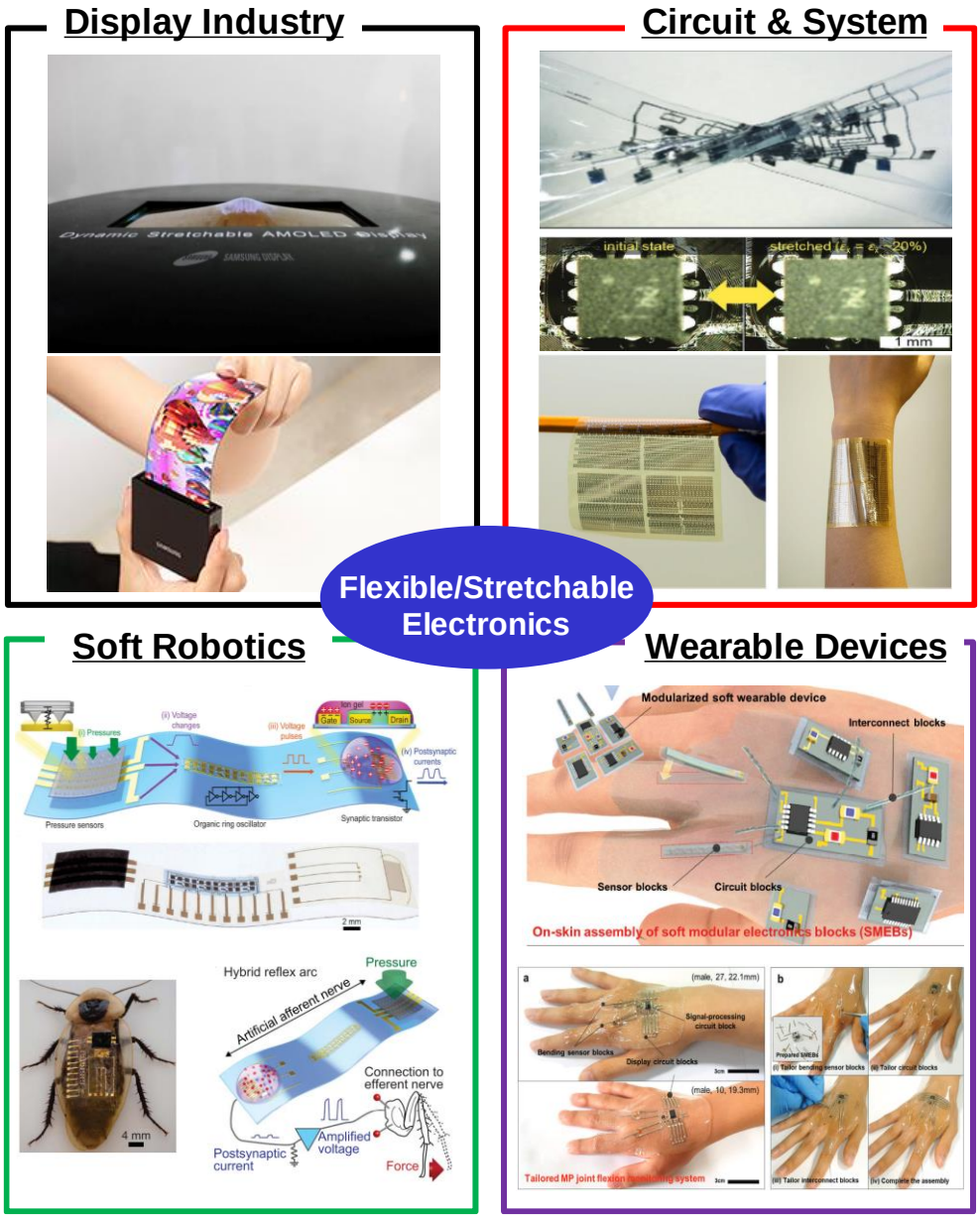

Figure 1.1. Various examples of flexible/stretchable electronic applications, such as display industry (Source: Samsung Display), circuit and system [1-2], soft robotics [3], and wearable devices [4], for next-generation.

solution-process. In conventional fabrication of TFT, vacuum-process based on high-vacuum environment with lithography patterning has been widely used, including thermal evaporation, atomic layer deposition (ALD), and chemical vapor deposition (CVD) method. The device fabricated from these high-vacuum-based process exhibits much higher uniformity and electrical performance due to the low contaminations and defects during the fabrication compared with the one from the solution-process. However, it is very time-consuming process because high gauge level of vacuum is needed to deposit the high-quality thin films of each layer of TFT, and it is high-cost and complicated process because multiple photo-masks are needed for patterning the each layer of the device. Furthermore, a usage of toxic gases and various solvents in photoresist at multiple patterning processes adds the process complexity and the cost. These disadvantages of the vacuum-process make it hard to implement the flexible and stretchable electronic applications. In contrast, although the device fabricated from the solution-process including spin-coating or inkjet-printing exhibits relatively low electrical performance and uniformity compared with vacuum-processed one, the solution-process has been received great attention from many engineers due to its low-cost and low-temperature processability that can make it possible to realize the facile implementation of flexible/stretchable electronics systems [8-13]. Differences between vacuum-process and solution-process mentioned in this chapter 1.1 are summarized in table 1.1.

	Solution-process	Vacuum-process
Advantages	✓ Low-cost fabrication ✓ Low-temperature fabrication ✓ Fast/Facile fabrication	✓ High performance ✓ High uniformity ✓ Low contamination during fabrication
Disadvantages	✓ Low performance ✓ Low uniformity	✓ Complex and time-consuming fabrication ✓ High-cost fabrication
Examples	✓ Spin-coating ✓ Inkjet/gravure printing	✓ Atomic layer deposition ✓ Chemical vapor deposition

Table 1.1. Differences between solution-process and vacuum-process**.**

1.2. Solution-processed Single-walled Carbon Nanotube Transistor

Referring to the chapter 1.1, solution-processed thin-film transistor has considerably attracted a lot of attention because it is a promising device to meet the demand for various electronic applications such as wearable sensor and flexible/stretchable display due to its low-temperature and low-cost processability. Accordingly, various solution-processable active materials, for example, organic, metal-oxide, and carbon-based materials, have been investigated [14-20]. Among them, solution-processed single-walled carbon nanotube (SWCNT) material has been widely studied due to its various advantages that can be potentially applied to the next-generation electronic applications. Therefore, in this chapter 1.2, I briefly introduce the semiconducting SWCNT and its advantages, and then various deposition methods of it based on the solution-process will be followed.

1.2.1. Semiconducting Single-walled Carbon Nanotube

Carbon nanotube (CNT), which was firstly discovered in 1991, consists of single-walled carbon nanotube (SWCNT) and multi-walled carbon nanotube (MWCNT). SWCNT is a cylinder structure up which a one-atom thick layer of graphite (called graphene) is rolled, and MWCNT is the arrays of multiple SWCNTs (Figure 1.2a, 1.2b) [21-23]. In SWCNT, mechanical structures and characteristics of nanotube are determined by rolling directions of graphene. These directions can be defined with a pair of basis vector ($\mathbf{a}_1$, $\mathbf{a}_2$) and integer (n, m),

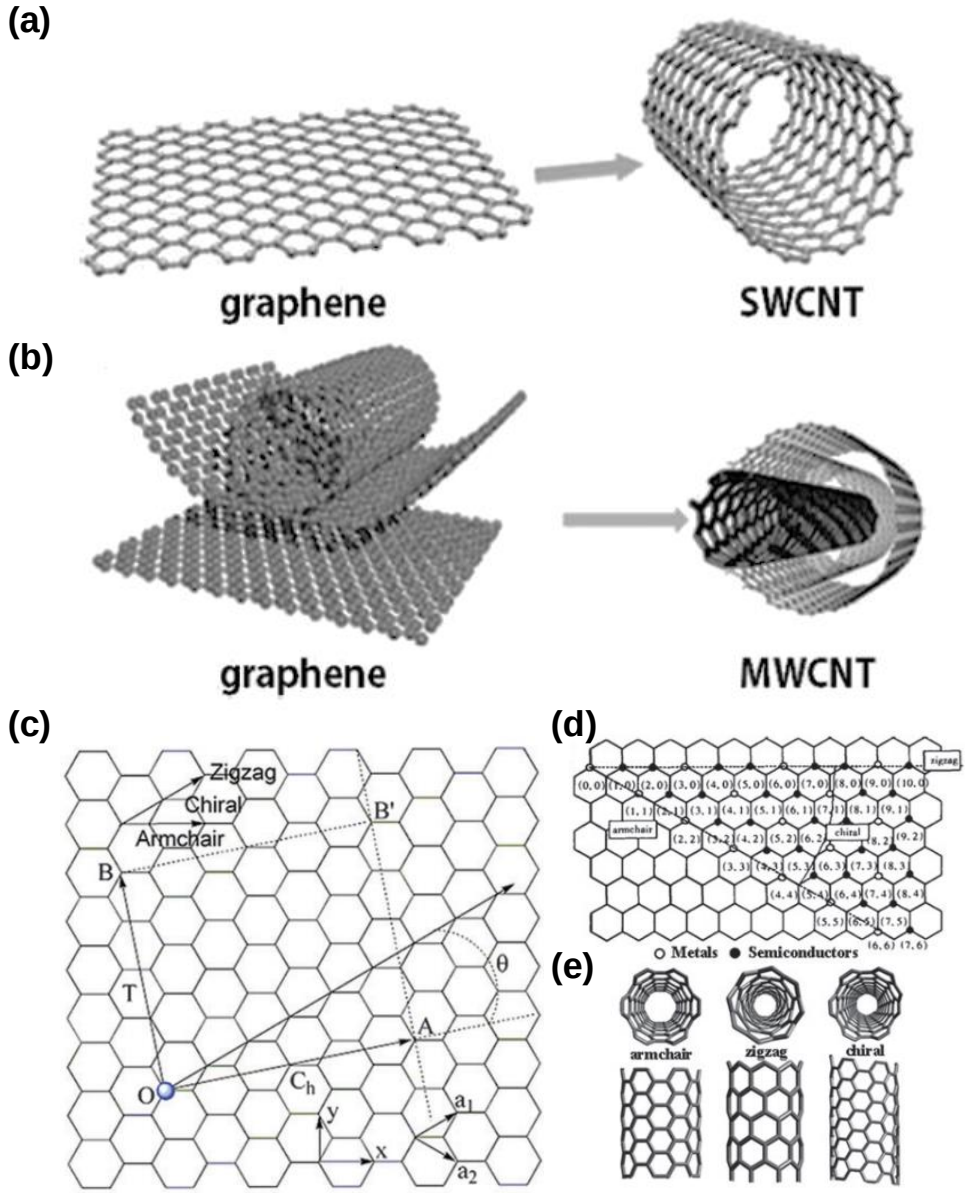

Figure 1.2. Structure of (a) SWCNT and (b) MWCNT from the graphene [22]. (c) Schematic image of chiral vector in graphene. (d) Dependency between chiral vector (n,m) and electrical nature of SWCNT (metallic and semiconducting). (e) Three different structures of SWCNT depending on the pair of integer (n,m) [25].

which is called the “chiral vector” ($C = n\mathbf{a}_1 + m\mathbf{a}_2$). Specifically, the nanotubes with the integer m value of 0 are called “zigzag”, and the nanotubes with the integer m value of n are called “armchair”, and other angular states are called “chiral”. And, based on the relationship between the two integers (n,m), electronic nature of these SWCNTs, which is metallic or semiconducting, is determined. When $|n-m| = 3k$ (k is an integer), the tubes exhibit metallic property, whereas the other cases are semiconducting property. For example, nanotube with the integer pair of (4,1) exhibits the metallic property (Figure 1.2c-e) [24,25]. Figure 1.3 shows the band-diagram structure and related density of state (DOS) of each case (metallic and semiconducting) of SWCNT, and discontinuous series peaks in the density of state at the SWCNT shown in figure 1.3 are known as van Hobe singularities [26,27].

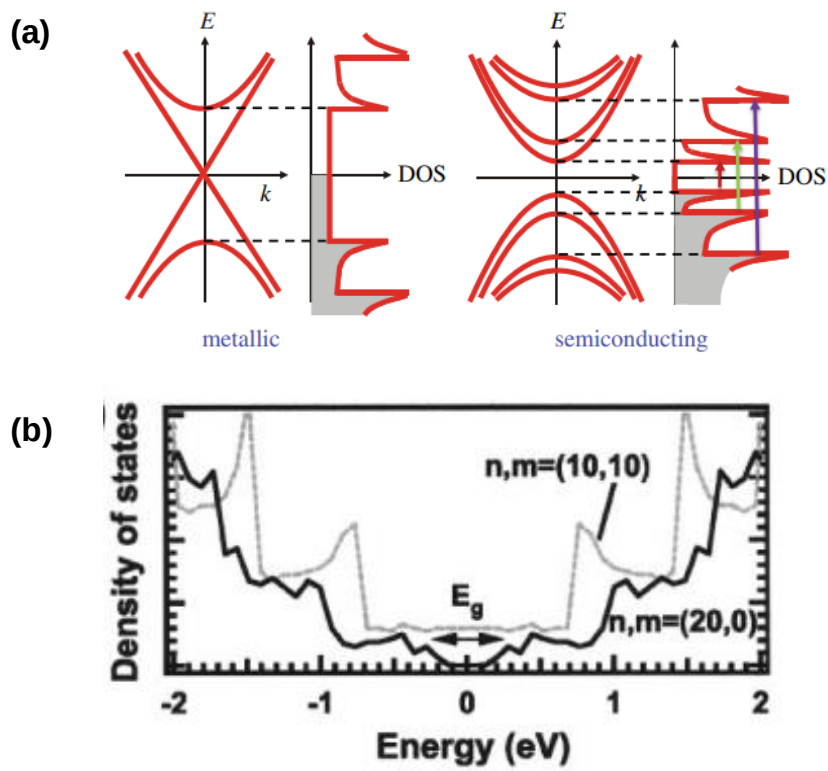

Figure 1.3. (a) Energy band diagram and (b) density of state in case of semiconducting and metallic SWCNTs. (In figure (b), (10,10) is metallic SWCNT, and (20,0) is semiconducting SWCNT.) (reference : (a) [26], (b) [27])

In particular, the SWCNT exhibits various extraordinary mechanical, electrical, and optical properties as follows, which is the reason why many people choose it to study including my researches: (i) It has remarkable mechanical properties. SWCNT has high tensile modulus (about terapascal (TPa) range), so that the material itself has high strength and stiffness in the mechanical stress [28,29]. These advantages can facilitate the implementation of intrinsically stretchable electronic applications based on the SWCNT for the wearable industry. (ii) It has remarkable electrical properties. The SWCNT exhibits high intrinsic carrier mobility (above 10^4 cm^2/Vs) for the generation of high-current level. Furthermore, small diameter (about nanometer scale) of the SWCNT can reduce the operating voltage of the device due to easy controllability of thin-film of it [30,31]. Aforementioned electrical characteristics of the SWCNT are comparable or even much better compared with those of silicon-based or other types of transistor, so it can be possible to utilize the SWCNT material for implementing the electronic devices that require the high-performance and low power consumption. (iii) It has remarkable optical properties. Thin-film of SWCNT can exhibit high transparency, so that the demand for transparent devices is much easier to be satisfied with it [32].

Furthermore, as the technologies of purifying the semiconducting SWCNT from the metallic one have been constantly developed like density gradient ultracentrifugation (DGU), dispersed ink of highly-purified semiconducting SWCNTs is easily produced and widely commercialized for implementing the large-area flexible and stretchable electronic applications, for example, logic circuits, active-matrix panel, and biosensor array, because it is

possible to fabricate the device at the low-temperature and low-cost based on the solution-process. Consequently, there are many extensive previous researches about the solution-processed SWCNT TFT and its application for the flexible/stretchable electronics [33-40].

1.2.2. Various Deposition Methods of Semiconducting SWCNTs with Solution-process

To implement the reliable large-area SWCNT TFTs array based on the solution-process, various deposition techniques of semiconducting SWCNTs have been employed. Typically, these can be divided into three main categories, which are direct deposition, direct printing, and self-assembly method. Direct deposition method including dipping and drop-casting is that the substrate is directly immersed into the SWCNT solution or the ink is dropped all over the substrate, resulting in whole deposition of SWCNTs onto the target substrate [36,41]. Direct printing method including inkjet and gravure printing is that the thin-film of SWCNT is selectively deposited at the desired region by using many types of printer device, which has great advantages for economical material usage and eliminates the need for additional patterning process [42,43]. Self-assembly method is that the SWCNT network is deposited by the fluidic mechanism between the SWCNT ink and the target substrate. Unlike the other two methods that form the random network of SWCNT at the channel region, this method can be possible to make the aligned network of SWCNT at the channel region for the better performance of device [44]. Representative illustrations based on the previous reported researches of each case are shown in figure 1.4.

Among them, direct deposition method exhibits the greatest advantages for the device implementation at the large-area for electronic applications because it features low process complexity, high uniformity over large-area, and low degree of contamination compared with other deposition methods. Other two methods, however, exhibit some disadvantages for the commercialization of those electronics. In direct printing method, coffee-ring effect is generally the main issue of the printing technology because it can act as a defect and also can degrade the electrical performance and uniformity of the devices. And in self-assembly method, although the high-performance device can be obtained due to the densely aligned SWCNT network, process controllability is very hard to commercialize, and large-area scalability and fabrication throughput are very low. Characteristics of each deposition technique from the various points of view, such as the process complexity, uniformity at large area, degree of contamination, and throughput, are summarized at table 1.2 [45,46]. For these reasons, therefore, many research groups have employed the direct dipping method to implement the backplane for the various applications at large-area such as active matrix backplane for pressure mapping and driving for OLED device (Figure 1.5) [36,47].

Table 1.2. Characteristics of each deposition technique: (i) Direct deposition method, (ii) Direct printing method, (iii) Self-assembly method.

	Direct dipping method	**Direct printing method**	**Self-assembly method**
Process complexity	Low	Medium	High
Uniformity (@ large area)	High	Low	Medium
Degree of contamination	Low	High	Low
Throughput	High/Low	High	Low
Network	Random network	Random network	Aligned network
Examples	Dipping Drop-casting	Gravure printing Inkjet printing	-

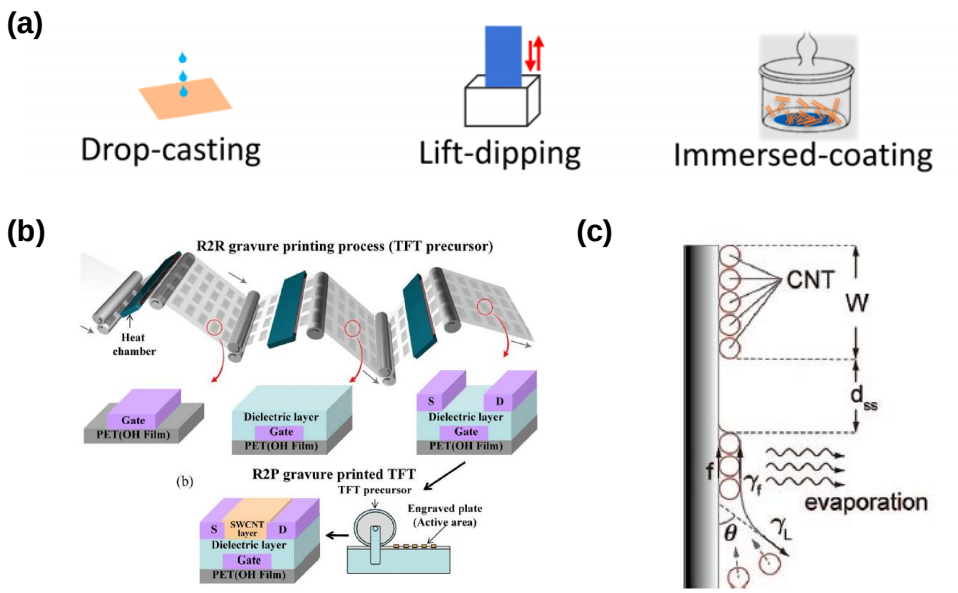

Figure 1.4. Representative illustrations of three different deposition methods of semiconducting SWCNT based on the solution-process expressed in previous researches: (a) Direct dipping method (drop-casting and immersing) [48], (b) Direct patterning method (gravure printing) [43], (c) Self-assembly method [44].

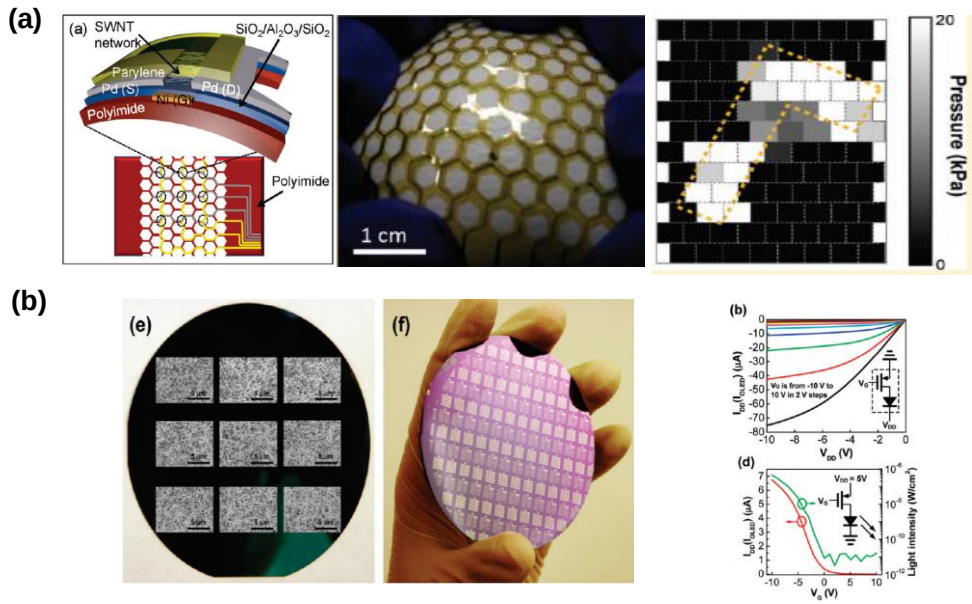

Figure 1.5. Previous researches about the implementation of large-area SWCNT TFT array based on direct deposition (dipping or immersing) method for (a) active matrix backplane for pressure mapping [36], and (b) driving circuit of OLED [47].

1.2.3. Main Issues of Direct Dipping Methods

However, when the SWCNT TFTs are manufactured by the direct dipping method, fabrication yield is generally low due to very long deposition time of SWCNT, especially with aqueous SWCNT ink, and additional patterning process is needed. Total required time for depositing the active layer with dipping of semiconducting SWCNT is from a few hours to several days with aqueous SWCNT solution, which can cause the low yielding ratio of the device fabrication [45,46]. Furthermore, additional patterning process, such as oxygen plasma etching with patterned mask or physically isolating, is required after the deposition of SWCNT, as non-patterned SWCNT can cause additional leakage current path to

the TFT device at off-state. However, this additional process cannot be suitable for future roll-to-roll (R2R) process or large-area fabrication because it could not only damage other circuit elements of the device but also increase the complexity of process and the cost, so that the limitations when customizing the various patterns are followed [49,50]. Therefore, these limitations can disturb the further development of future industries based on the SWCNT TFT fabricated with the direct dipping method for the various applications in real life.

1.3. Organization of this thesis

In this dissertation, therefore, each following chapter will introduce the two newly developed strategies, which are “Multi-dipping technique” (chapter 2 in this thesis), and “Inkjet-printing of surface treatment materials (Poly-l-Lysine, PLL) technique” (or “self-patterning technique”, chapter 3 in this thesis), for resolving the issues of direct dipping methods mentioned in chapter 1.2.3. After that, verification process of applicability of these two techniques for implementing the high-throughput and high-resolution SWCNT TFT will be presented. Specifically, I checked the applicability based on the criteria of large-area scalability and micro-patternability (chapter 4 in this thesis). All chapters include the introduction of the main concept, experimental methods, and series results and discussions about the experiment. In particular, all chapters are based on an as-purchased aqueous SWCNT ink, and whenever I purchased the SWCNT inks (95% semiconducting, Nanointegris Corp.), the chemical conditions of the ink were a little or a lot different, so corresponding process conditions were always re-optimized. Schematic of the storyline of this thesis is summarized at figure 1.6.

This dissertation contains five chapters, including the introduction (chapter 1) and summary (chapter 5) part. Detailed explanations of each chapter are as follows:

Chapter 1 briefly introduces the overall explanation of solution-processed thin-film transistors and single-walled carbon nanotube. Then, various deposition methods of semiconducting SWCNT based on the solution-process with their pros and cons are followed. Among them, direct dipping method is one of the most suitable candidate to implement the next-generation large-area flexible/stretchable

electronic systems due to its scalability and facile controllability. However, some limitations of it exist and are needed to be resolved, which is the core theme of this dissertation.

Chapter 2 introduces the “Multi-dipping technique” to rapidly form high quality film of random network of semiconducting SWCNT used as a channel material. This technique is developed to solve the long deposition time of direct dipping method. This chapter explains the concept and method of the multi-dipping technique for reducing the deposition time of SWCNT. By introducing the multi-dipping technique, not only did the total fabrication time of device remarkably decrease, but also the electrical performance of the device was improved at the same time. In addition, deposition mechanism of the multi-dipping technique is introduced with comprehensively analyzed results of atomic force microscopic (AFM) image inside the channel region.

Chapter 3 introduces “Inkjet-printing of PLL technique” (or “self-patterning technology of semiconducting SWCNT”) to *in-situ* self-pattern the solution-processed and directly deposited random network of SWCNT. Only with the developed PLL printing technique, semiconducting SWCNTs were successfully *in-situ* self-patterned only at the channel region without any additional patterning process. This chapter explains the concept and the optimization process of inkjet-printing the PLL for the *in-situ* patterning of SWCNTs. By employing the technique with fully optimized conditions, the SWCNTs were only patterned at the patterned region of surface treatment material where we want to deposit them without any issues. After that, detail explanations about the successful implementation of SWCNT TFTs array with the PLL patterning technique at the Si/SiO_2 substrate are followed.

Chapter 4 introduces the definition of integration of the aforementioned newly developed two techniques, which is defined as “Fast and self-patterning technique”, then the verification process of feasibility and applicability of the integrated technique based on the viewpoint of large-area scalability and micro-patternability is followed. First, the former one was verified by implementing 8 x 8 SWCNT TFTs array with two techniques at 2 cm square Si/SiO_2 substrate and examining the throughput and electrical performance of the array. And, the latter one was verified by demonstrating all-electrohydrodynamic (EHD)-printed SWCNT TFT with the integrated one onto the glass substrate. In the second verification process, EHD technique is introduced and utilized to effectively emphasize the micro-patternability of fabricated TFT due to its remarkable ability to minimize the size of printed patterns. And this chapter summarizes the reason why my fast and self-patterning technology can be suitable for next-generation large-area flexible/stretchable electronic applications.

Chapter 5 finally summarizes the achievements of the dissertation with some limitations and related works. Furthermore, the roadmap for future researches and other engineers in the field of electrical and display engineering based on this study is discussed and recommended with overall storyline of this dissertation and future trends.

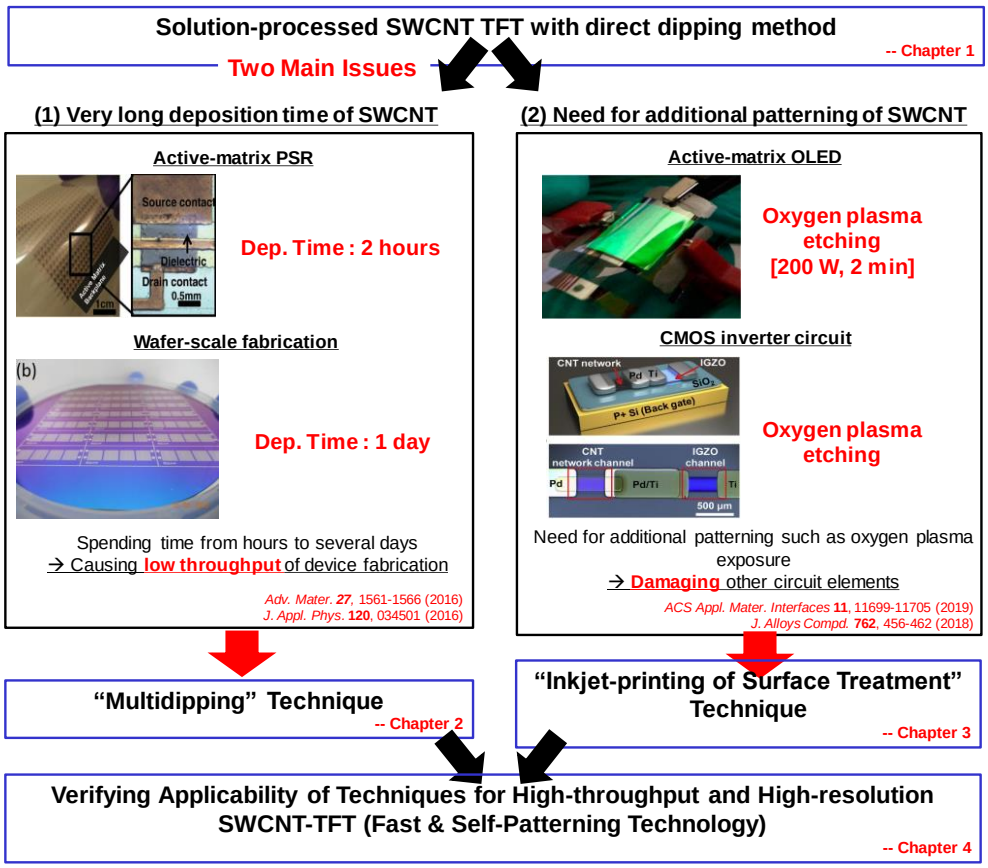

Figure 1.6. Schematic of the storyline of this thesis (reference : [20], [49-51]).

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Chapter 2

Multi-dipping Technique of Semiconducting Single-walled Carbon Nanotubes for Rapid Fabrication and Performance Improvement of Solution-processed TFTs

2.1. Introduction

As mentioned in introduction chapter, many research groups have pointed out that the fabrication throughput is generally low when the SWCNT TFTs are fabricated with the direct dipping method due to a very long deposition time of SWCNT, especially with aqueous SWCNT solution [1-3]. It is noted that various surfactant materials, such as sodium dodecylbenzene sulfonate (SDBS), sodium dodecyl sulfate (SDS), sodium cholate (SC), are generally used to form well-dispersed aqueous SWCNT solution with long-term dispersion stability. Among them, although steroid-chain-based surfactants do not hinder the attachment of semiconducting SWCNT onto the surface, they degrade the dispersion quality of

the aqueous SWCNT solution. On the contrary, alkyl-chain-based surfactants like SDBS and SDS, widely used for effective additives at the commercially available SWCNT ink, generally counteract against the formation of SWCNT, and repulsive force caused by them makes the deposition time much longer though the quality and stability of dispersion are improved [1,4-5]. The more stable the ink is, the longer the deposition time is (Figure 2.1).

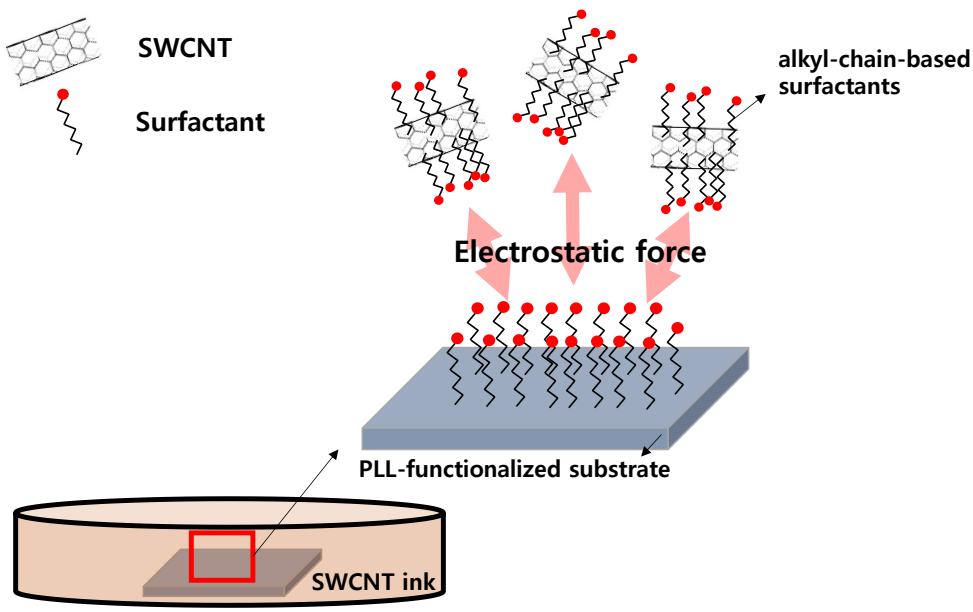

Figure 2.1. Principle of direct dipping method of semiconducting SWCNT with aqueous SWCNT solution.

Therefore, in my group's previous research, the total deposition time of SWCNTs was significantly reduced by adding certain amounts of diluted acid into the as-purchased aqueous SWCNT ink with controlling the pH of the solution. As the addition of diluted acid decreases the pH and modifies the zeta-potential of the dispersed solution, it reduces the repulsive force caused from the surfactants. However, the dispersion stability of the ink could be degraded as the pH of the solution is lowered because ionic surfactants attached at SWCNT are modified, which can make the SWCNTs in the ink or at the network film on the substrate aggregated [1]. These aggregations of SWCNTs, however, could not be suitable for short channel device whose length is similar scale to the length of nanotube (a few micrometers). Another way to reduce the deposition time of SWCNT film is using SWCNT ink dispersed in organic solvent such as N,N-dimethylformamide (DMF) and 1-methyl-2-pyrrolidone (NMP). With this method, electrostatic repulsive force caused from the surfactants is not needed to be considered because the surfactants are not necessary when dispersing the SWCNT in organic solvent. However, this method is not suitable for implementing the flexible or stretchable electronic applications because the organic solvent could chemically attack some polymeric substrates and dielectrics for TFT devices [6-8].

In this chapter 2, I implemented a simple and effective technique, which is "multi-dipping" technique, in order to rapidly form a dense and high-quality SWCNT film at the channel region with a short deposition time. Unlike conventional dipping technique, which is called "one-time dipping" where the substrate is dipped only once in SWCNT ink with a very long deposition time, in multi-dipping technique, the substrate is repeatedly dipped in SWCNT ink for a very short deposition time during each dipping process and rinsed between the

multiple dipping steps. By applying the newly desired multi-dipping technique, not only was the deposition time of SWCNT significantly reduced, but also the electrical characteristics of the TFT devices were improved, and moreover, the dispersion stability of the original solution did not degrade. And I comprehensively analyzed the deposition mechanism of multi-dipping technique with AFM image inside channgel region in this chapter.

2.2. Experimental methods

2.2.1. Fabrication Process

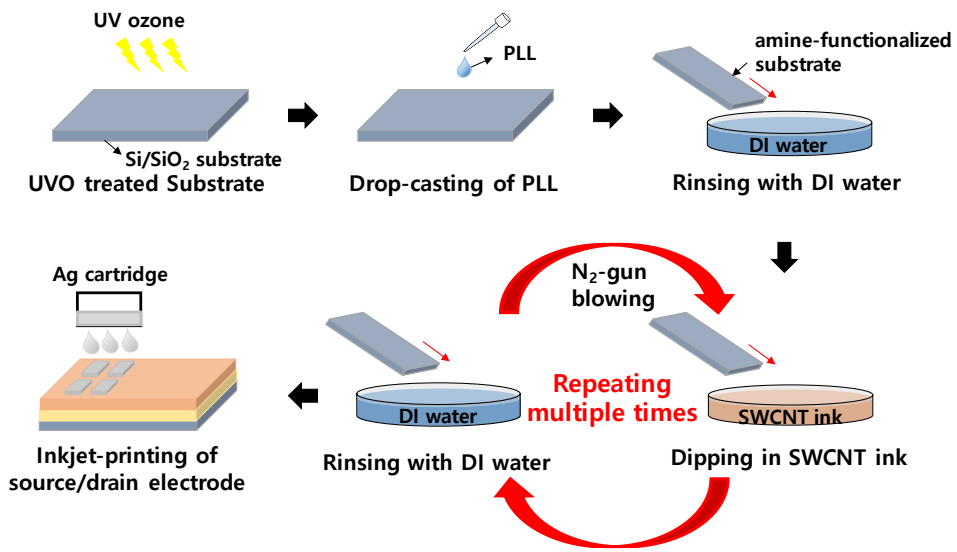

Figure 2.2. Overall fabrication process of SWCNT TFTs with multi-dipping technique.

Figure 2.2 shows the overall fabrication process of SWCNT TFTs with the multi-dipping technique. First, heavily doped p-type Si (thickness of 550 μm) with thermally grown SiO_2 (thickness of 200 nm) wafer was used as a gate electrode and gate dielectric, respectively. For fabricating the device, the wafer was sequentially rinsed with acetone and isopropyl alcohol (IPA) for 20 minutes in ultrasonic bath for each solvent, blown with nitrogen (N_2) gun, and baked in oven at 100 ˚C for 40 minutes. Then the wafer was exposed with ultraviolet ozone (UVO) lamp in chamber for 10 minutes to form hydroxyl group (-OH) on its surface. After that, to

easily attach the semiconducting SWCNT onto the substrate, poly-L-lysine (PLL) solution (aqueous solution, 0.1% (w/v) in H_2O, Sigma-Aldrich corp.) was drop-casted for 10 minutes on the UVO-treated substrate, and it was rinsed with deionized (DI) water for one minute and blown with N_2-gun to form the amine-functionalized surface on the wafer. In one-time dipping method, the amine-functionalized substrate was dipped into as-purchased 95% semiconducting-enriched SWCNT ink for a very long time, rinsed with DI water for one minute, and blown with N_2-gun. Rather, in multi-dipping method, the functionalized wafer was dipped into SWCNT ink for one minute, rinsed and blown with the same recipe, and this procedure was iterated many times to form the high-quality networks in the channel area. On the SWCNT layer, source and drain electrodes were inkjet-printed with a piezoelectric type inkjet-printer (DMP-2831, Dimatix Corp.) by using metal-organic based silver ink (JET-004T, Kunshan Hisense Electronic Corp.), and the substrate was sintered with hot-plate at 130 ˚C for 30 minutes. Used piezoelectric type inkjet-printer and camera image of ink-drop of silver in this chapter are shown in figure 2.3. TFTs with the bottom gate and top contact structure were formed as shown in figure 2.4a. Figure 2.4b shows the optical image of the channel region with the inkjet-printed source/drain Ag electrodes. Length (L) and width (W) of the channel were 160 μm and 180 μm, respectively. More than 10 devices were fabricated on a 2 cm square wafer, and the SWCNT film of each device was physically isolated using a hard tip to remove unnecessary current path.

2.2.2. Measurement Details

Electrical characteristics of the SWCNT-TFTs such as transfer and output curves were measured with agilent 4155C semiconducting parameter analyzer. And the optical images of channel region were obtained with optical microscope (DSX510, Olympus Corp.). Morphology of channel regions were analyzed with AFM equipment (XE-100, Parks' System Corp.).

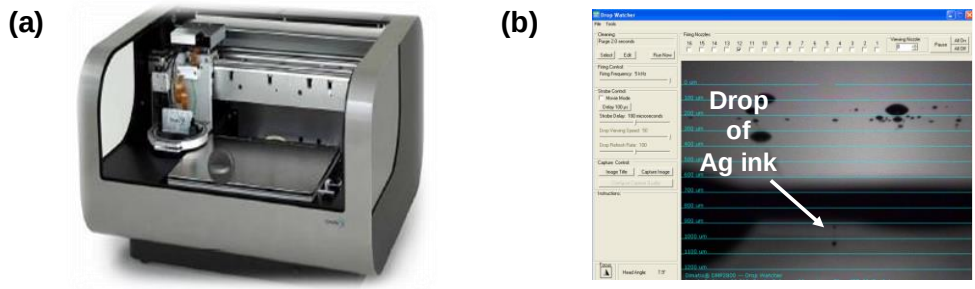

Figure 2.3. (a) Camera image of inkjet-printer (Source : Dimatix Corp.). (b) Camera image of ink-drop of metal-organic based silver ink (JET-004T).

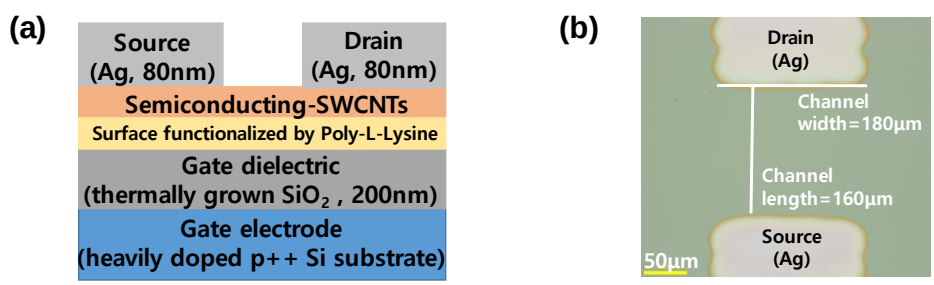

Figure 2.4. (a) Cross-section view of fabricated SWCNT TFT structure. (c) Optical image of device channel region with inkjet-printed source and drain Ag electrode.

2.3. Results and Discussion

2.3.1. Comparison of Fabrication time and Electrical Performances of SWCNT TFT

Figure 2.5a exhibits the measured transfer characteristics of the fabricated TFTs, and figure 2.5b exhibits the transfer characteristics of representative data of each case, which has very similar on-current level between one-time dipping and multi-dipping. In case of multi-dipping method, density of SWCNTs in the channel area depends on the number of iteration, while it depends on the deposition time in the one-time dipping method. As shown in figure 2.5, significantly long deposition time was required to observe a reasonable TFT performance in the one-time dipping method for the as-purchased SWCNT ink. It is noted that the as-purchased ink has a large amount of surfactants for dispersion quality and longer dispersion stability, and thus it takes unexpectedly long time to obtain dense SWCNT network in the channel area. In contrast, short deposition time of SWCNT was needed to achieve similar on-current level in multi-dipping method (for example, 750 minutes versus 1 minute x 30 times for similar on-current level). Especially in case of 35 times of multi-dipping, it took about 82 minutes to totally fabricate the active layer when considering the time of dipping (1 minute), rinsing with DI water (1 minute), and N_2-gun blowing with handling (20 seconds) in each step. The aforementioned case of multi-dipping, however, still exhibited over time reduction of 90% compared with the case of 1080 minutes of one-time dipping. Therefore, these results clearly show that the multi-dipping method significantly reduced the

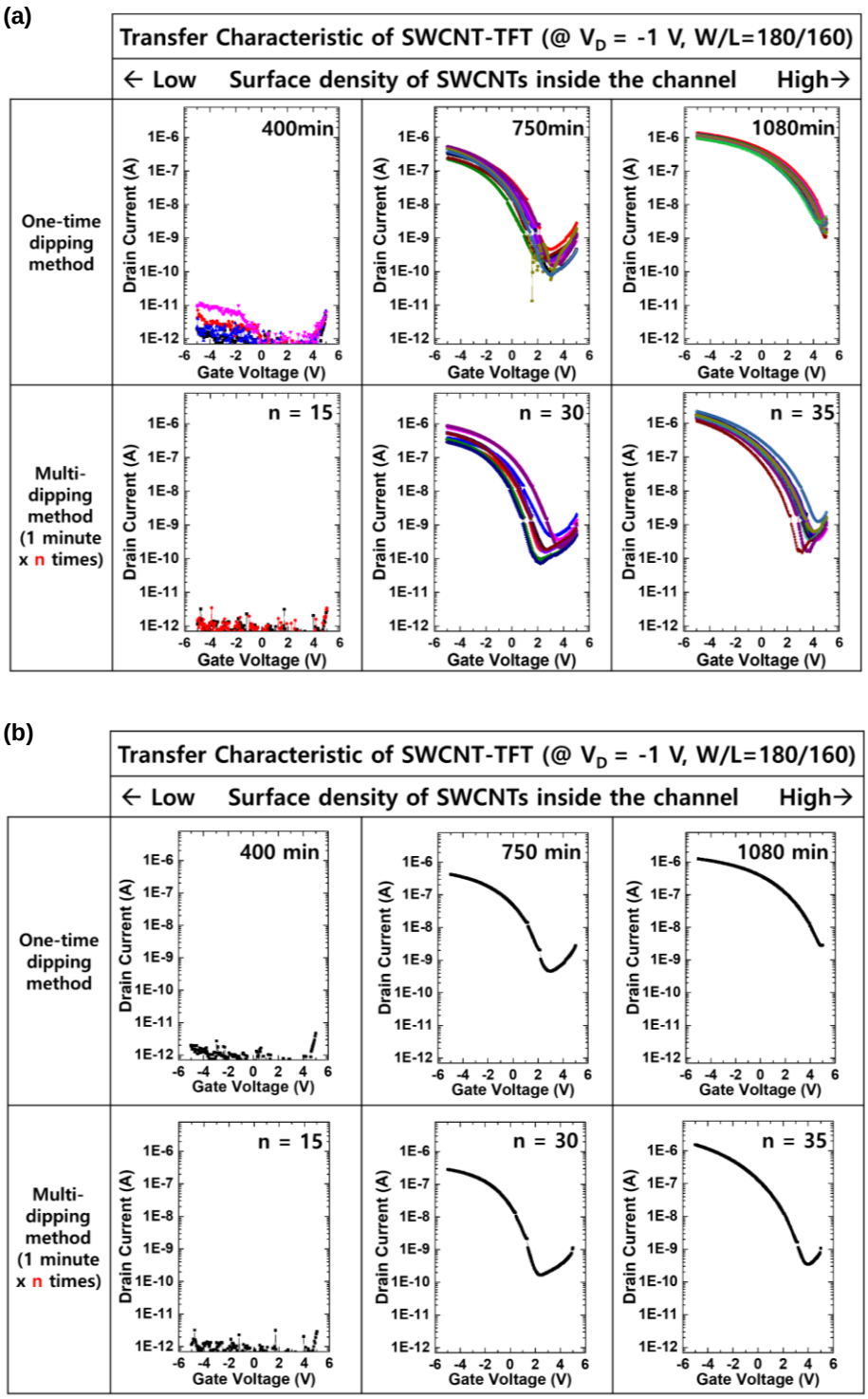

Figure 2.5. (a) Transfer characteristics of devices depending on the densities of SWCNTs which is controlled by dipping time at one-time dipping and iteration time at multi-dipping method. (b) Representative data from figure 2.5a, which exhibits almost same on-current level.

total time for device fabrication, even though I simply considered the repetition of 1-minute dipping and rinsing steps.

Figure 2.6 exhibits the the transfer, hysteresis, and output characteristics of unit device of one-time dipping of 1080 minutes and multi-dipping of 35 times. Field-effect mobility (μ), subthreshold swing (S.S.), and turn-on voltage ($V_{turn\text{-}on}$) were extracted from the transfer characteristics measured at forward sweep (from positive to negative) of gate bias since the nanotube transistors usually exhibit the p-type characteristic in ambient condition. For calculating the value of field-effect mobility in all chapters including chapter 2, I used a conventional extraction method of field-effect mobility (max-g_m method) based on simple-parallel model (as shown in Figure 2.7b). It can be possible to consider the nanotube network inside the channel region, which is quantum capacitance, when extracting the mobility. However, as the value of quantum capacitance is higher than the capacitance generated by gate dielectric, the gate capacitance is dominant since the two capacitances are in series. Therefore, many related researches used the simple-parallel model for extraction as I used [9,10]. Table 2.1 summarizes the extracted parameters of the device for the case of the highest density of SWCNTs in figure 2.5 (specifically, 1080 minutes in one-time dipping versus 1 minute x 35 times in multi-dipping). For as-purchased ink, when the devices were fabricated with the multi-dipping method, the mobility was increased, and turn-on voltage and subthreshold swing were decreased in comparison with those made from the one-time dipping method. So, I can insist that the electrical performance of the device fabricated with multi-dipping is much higher compared with that of the device fabricated with one-time dipping.

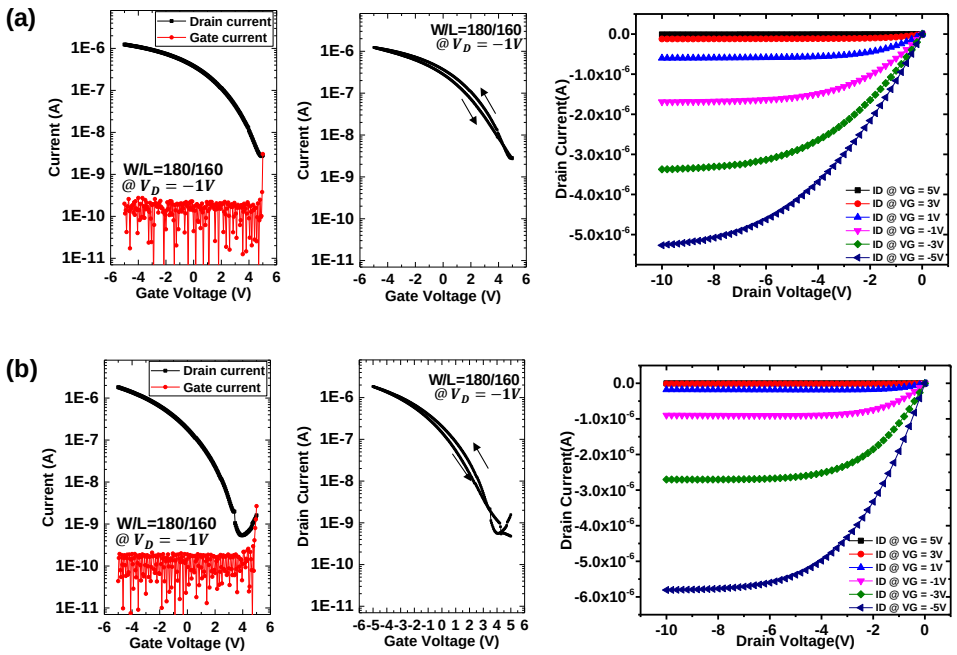

Figure 2.6. Transfer, hysteresis, and output characteristics of unit device of (a) one-time dipping device (1080 minute) and (b) multi-dipping device (1 minute x 35 times).

Type	Mobility [cm^2/Vs]	Turn-on voltage [V]	S.S. [V/dec]
(a) As-purchased, one-time dipping **(1080 minute)**	**9.02 ± 0.85**	**4.77 ± 0.22**	**1.35 ± 0.20**
(b) As-purchased, multi-dipping **(1 minute x 35 times)**	**20.74 ± 2.41**	**3.83 ± 0.31**	**1.06 ± 0.12**

Table 2.1. Summarized extracted parameters of devices in case of one-time dipping (1080 minutes) and multi-dipping (1 minute x 35 times) shown in figure 2.5a.

2.3.2. Mechanisms of SWCNT Network Formation

Overall the chapter 2.3.1, multi-dipping method can significantly reduce the total deposition time of SWCNT and enhance the electrical performances of the TFT device at the same time with the as-purchased SWCNT ink, which is summarized in figure 2.7.

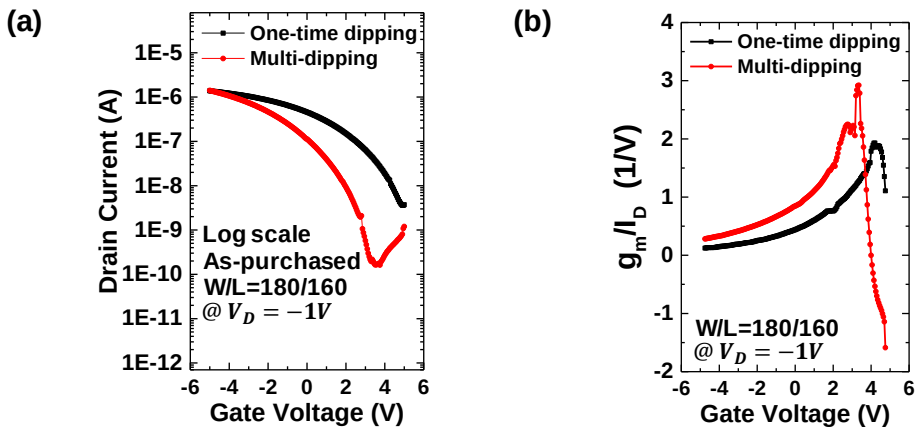

Figure 2.7. (a) Transfer characteristics and (b) their g_m/I_D-V_G curve of devices which have almost same on-current level between one-time dipping and multi-dipping devices fabricated with as-purchased SWCNT ink (1080 minutes; 35 times) plotted in one graph.

It is noted that deposition mechanism of SWCNT with dipping method is closely related with the electrostatic interaction between the amine-functionalized surface and SWCNTs [1,5]. The residue of the ionic surfactants attached to the amine-terminated substrate and pre-formed SWCNT layer, which is mixed in commercialized SWCNT ink in order to promote its dispersion stability, causes the repulsive force that can counteract to the further deposition of the SWCNTs during the dipping process between the residue and SWCNTs. As a result, the deposition time of SWCNT gets longer with the amount of ionic surfactant in as-purchased

SWCNT ink, and moreover, bundled SWCNT network is formed on the substrate since the additional SWCNTs cannot be easily attached on the surfactant-deposited surface where SWCNTs were not pre-formed [11]. However, by doing multiple DI water rinsing of the substrate between each short-time dipping step of SWCNT in multi-dipping process, the total deposition time was significantly reduced for the as-purchased ink because it is well known that rinsing processes with various solvents after the deposition of SWCNT, such as DI water, IPA, and acetone, remove the residue surfactant and weakly attached SWCNTs on the substrate. For this reason, the multiple DI water rinsing during multi-dipping process can effectively suppress the counteraction of the residue surfactant at the amine-functionalized substrate and pre-deposited SWCNT film [12-14]. Consequently, we could not only form the dense and uniform SWCNT network on the substrate but also decrease the total deposition time of SWCNT by using the multi-dipping technique.

In order to further experimentally investigate the effect of multiple rinsing at each dipping step of the multi-dipping process, we fabricated two types of device, each of which is from the multi-dipping process with or without DI water rinsing at each dipping step. The only different thing is DI water rinsing was performed only after the last dipping step in the case of the multi-dipping without DI water rinsing. The other procedures of TFT fabrication and the number of iteration were the same in both cases. Figure 2.8 exhibits the transfer characteristics of the aforementioned two types of devices. Only the devices from the multi-dipping process with DI water rinsing showed a TFT behavior, while the ones from the multi-dipping process without DI water rinsing did not exhibit any TFT characteristics. In other words, dense enough SWCNT network for a proper TFT performance was formed

at the channel area for the former ones but not for the latter ones. Generally, it is known that devices with proper density of SWCNT (above the percolation threshold) could only exhibit the proper transistor characteristic. If the SWCNT films starts to be much thicker or much denser than aforementioned percolation threshold, the on/off characteristics of the SWCNT TFTs will be degraded due to the increase of the percolation paths through a large amount of the tube-tube junctions [15-17].

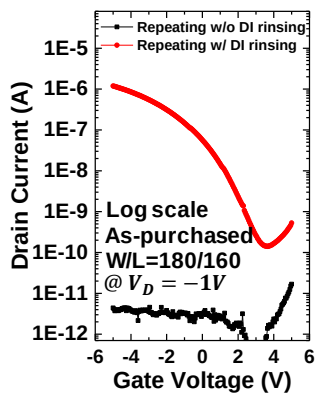

Figure 2.8. Transfer characteristics of devices which were fabricated with multi-dipping technique with and without DI water rinsing.

In multi-dipping without DI water rinsing process, even though the substrate is exposed to the air between each dipping step of SWCNT, the deposition mechanism is the same with the one-time dipping method because there is no repeated DI water rinsing between each dipping step. The residue of ionic surfactants at the amine-functionalized substrate and pre-formed SWCNT also remains in the case of multi-dipping without DI water rinsing process, so it hinders the additional attachment of SWCNT. However, it only takes 35 minutes (1 minute

x 35 times) to deposit the SWCNT in this case, so the overall deposition time of SWCNT is considerably short compared with the case of one-time dipping (1080 minutes). As a result, insufficient SWCNT network is formed in the case of multi-dipping without DI water rinsing compared with the case of one-time dipping. Therefore, from the result of multi-dipping with and without DI water rinsing, I can insist that repeated DI water rinsing between each dipping step of SWCNT is a key process of multi-dipping technique to make the dense, high-quality and sufficient SWCNT network inside the channel. The principles of three different dipping methods, which are one-time dipping, multi-dipping with DI water rinsing, multi-dipping without DI water rinsing, are summarized in figure 2.9. Case (i) exhibits the mechanism of one-time dipping, and case (ii) exhibits that of multi-dipping with DI water rinsing, and case (iii) exhibits that of multi-dipping without DI water rinsing.

It is possible, in multi-dipping technique, to further reduce the unit-dipping time for multi-dipping less than 1 minute as I set for reducing the total deposition time of SWCNT. However, I found that there would be an optimum unit-dipping time for given ink conditions of as-purchased SWCNT. The total fabrication time including the time of rinsing and blowing with handling could be ironically increased as the unit-dipping time is much shorter than the optimum time. In this case, effectiveness of multi-dipping can be degraded due to the difficult handling of consistent iteration of too short unit-dipping time, the re-increase of the total fabrication time, and negligible performance improvement caused from it. Therefore, in this chapter, the optimum unit-dipping time was set to 1 minute considering the total fabrication time, device performance, and repeatable process handling.

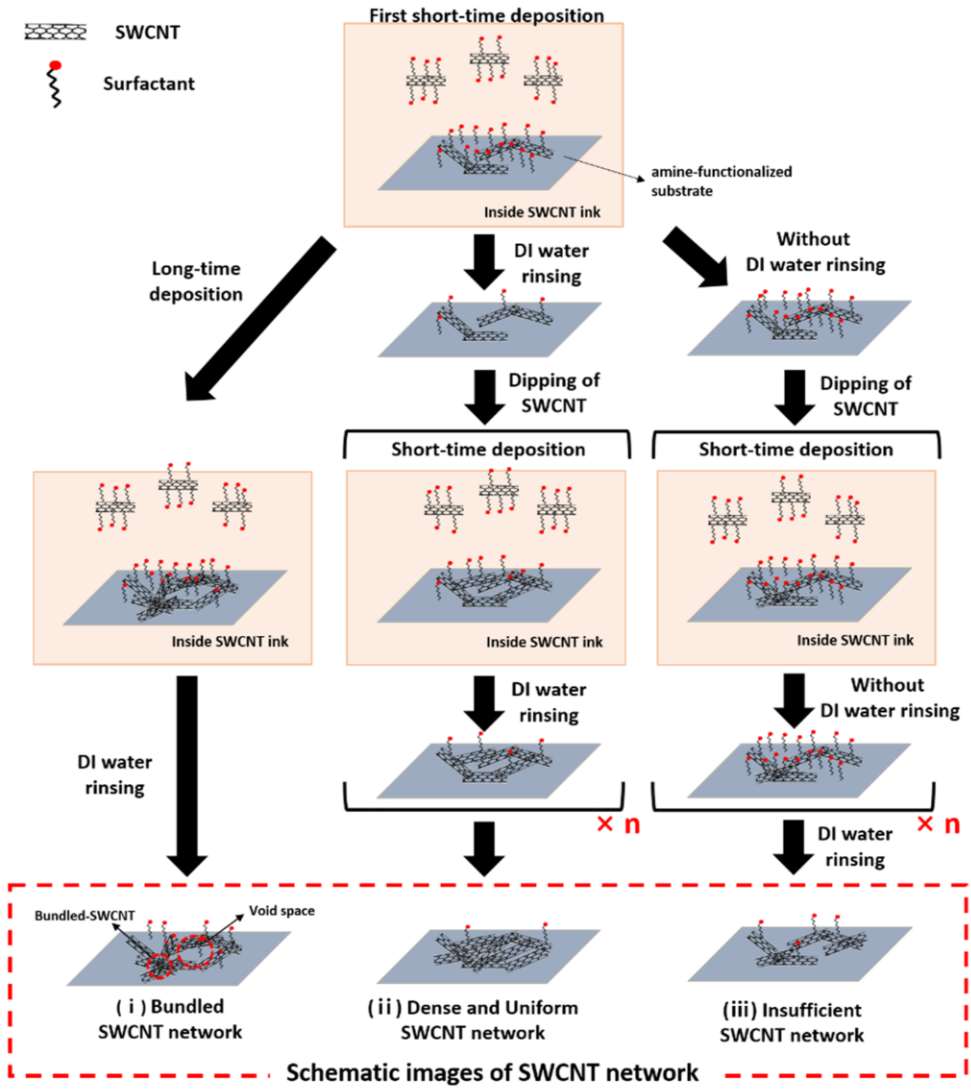

Figure 2.9. Illustration of deposition principle and fabricated SWCNT network of three different dipping methods, which are (i) one-time dipping, (ii) multi-dipping with DI water rinsing, and (iii) multi-dipping without DI water rinsing.

2.3.3. Channel Morphology

In this chapter 2.3.3, let me call the device fabricated with one-time dipping device A, the device fabricated with multi-dipping with DI water rinsing device B, and the device fabricated with multi-dipping without DI water rinsing device C. To verify the mechanism of SWCNT network formation of three types of dipping, I measured and analyzed the AFM images of the SWCNT film formed at the channel region of device A, B, and C. Generally in SWCNT TFT, the density and morphology of the SWCNT inside the channel region were analyzed with AFM images because these can efficiently show the morphology of random networks of SWCNTs inside the channel region [18,19].

Before discussing the AFM image, in optical images of device A and B (Figure 2.10), several impurities existed on the channel region. These are caused from the deposition of excess ionic surfactants in the solution and the bundles of SWCNTs during the dipping process, which can consequently degrade the electrical performance of the device [18]. By the way, in case of device B, the number of impurities in channel area was significantly reduced because the many times of DI water rinsing were performed during the multi-dipping process and the dipping time of SWCNT was significantly short compared with device A, which can be one of the reasons why the electrical performance of multi-dipping devices was improved. And in AFM images of these two cases (Figure 2.11a and 2.11b), void spaces between SWCNTs existed a lot in case of device A compared with device B. That means the random networks of SWCNTs are less compact and many bundled SWCNTs are formed on the substrate at the device fabricated with one-time dipping.

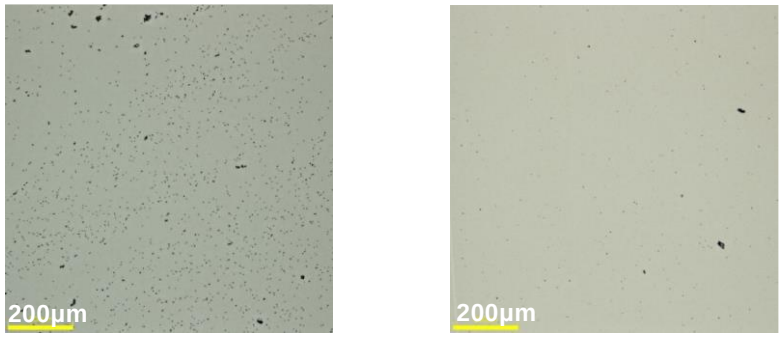

Figure 2.10. Optical images of channel region in case of one-time dipping (device A, left) and multi-dipping with DI water rinsing (device B, right) device.

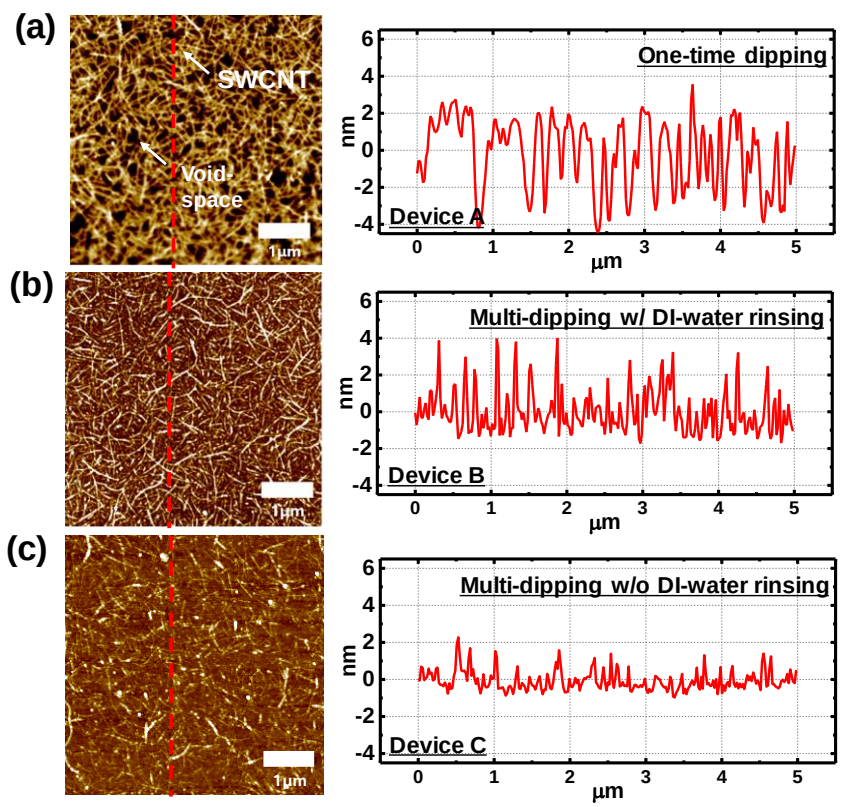

Figure 2.11. AFM images and line profiles extracted from red dotted line in AFM image of the channel region of (a) device A, (b) device B, and (c) device C.

From the AFM images in figure 2.11, I observed 8 profiles of channel area and extracted the root mean square (RMS) values of surface roughness and the peak-to-valley values from each profile to obtain the reliability of the extracted values. Among them, line profiles of red-dotted line in AFM images are shown in figure 2.11 for the case of device A, B, and C, and average full width at half maximum (FWHM) values from all peaks were extracted from them for effectively investigating the SWCNT bundle inside the channel network. Extraction method of FWHM value was based on the fitting of Gaussian distribution. The larger the average value of FWHM is, the more bundled SWCNT network exists inside the channel region [19]. All extracted parameters are summarized in table 2.2.

Type / Parameters	Device A	Device B	Device C
RMS value of surface roughness [nm] @ 8 lines	**1.83 ± 0.15**	**1.24 ± 0.11**	**0.65 ± 0.06**
Peak-to-valley value [nm] @ 8 lines	**8.80 ± 1.18**	**6.72 ± 0.11**	**3.64 ± 0.34**
Average value of FWHM [nm] @ line profile of figure 2.11.	**148**	**38.9**	**58.5**

Table 2.2. Extracted parameters from AFM profile in case of device A, B, and C.

In comparison between device A and B, there were many void space inside the SWCNT network and all extracted parameters exhibited much higher values in case of device A. It also means less compact and many bundled SWCNT network is formed in the channel area when depositing the SWCNT network with

one-time dipping method, while more densely and uniformly deposited SWCNT network is formed in the channel area when depositing the SWCNT network with multi-dipping method with DI water rinsing, resulting in much higher electrical performance of the device B. Generally, upper side of the SWCNT bundle can act as charge trap and increase the possibility of transferring the carrier charge between the source and drain electrode at off-state of the device, so that off-current level and turn-off voltage of the devices are even higher because of unwanted current path caused from these bundled SWCNTs [20-21].

In case of device C, less amounts of semiconducting SWCNTs were deposited and junctions between the SWCNTs were not enough to form the current path between the source and drain electrode on the substrate. Meanwhile, many SWCNTs were densely deposited at the channel area in case of device B (for example, 17 SWCNTs per 5 μm at red dotted line in device C versus 52 SWCNTs per 5 μm at red dotted line in device B.). These results also can be checked with the extracted parameters as shown in table 2.2 (device B versus device C). Only the average value of FWHM was slightly higher, and other parameters were relatively small in case of device C. That means insufficient but a little more bundled SWCNT network is formed when the film is fabricated with the multi-dipping without DI water rinsing.

Overall, all these results suggest that, in multi-dipping technique, multiple DI water rinsing at each dipping step is the core process to rapidly and densely deposit the SWCNT at the channel region, and based on this, devices from multi-dipping with DI water rinsing exhibit the best TFT performance with the time-saving fabrication.

2.4. Chapter Summary

In this chapter, simple and effective technique, which is “multi-dipping technique,” was demonstrated to rapidly form high quality random network film of semiconducting single-walled carbon nanotube (SWCNT) based on the solution-process. By applying the newly desired multi-dipping technique, the deposition time of SWCNT was significantly reduced, and moreover, the electrical performance of the fabricated TFT devices was enhanced at the same time with maintaining the dispersion stability of the original solution. In addition, deposition mechanisms of multi-dipping technique were comprehensively introduced and analyzed with AFM image of channel region. I believe this work can be easily applied for the facile implementation of flexible/stretchable electronic system based on solution-processed SWCNT TFTs.

Reference

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Chapter 3

Self-patterning Technique of Semiconducting SWCNT Based on Inkjet-printing of Surface Treatment Material

3.1. Introduction

As mentioned in introduction chapter, another issue of direct dipping method is the need of additional patterning steps, such as oxygen plasma etching and physical isolation, for reducing the leakage current path through unnecessary SWCNT outside the channel region [1-3]. However, these additional processes cannot be suitable for implementing the next-generation flexible/stretchable electronic applications based on SWCNT TFT due to these two reasons : (i) It can make other circuit or system elements damaged by UV light or air plasma. The damage of circuit, such as oxidation of electrode or degradation of dielectric, can cause the degradation of the device and circuit performance. (ii) It increases the fabrication complexity, because it needs more fabrication steps and some equipments like metal mask or isolation devices. Moreover, it is very hard to

fabricate various customized patterns at desired position with these pattern masks for various circuit applications.

Therefore, in chapter 3, I implemented facile *in-situ* self-patterning technique, which is "inkjet-printing of PLL technique," in order to selectively deposit the semiconducting SWCNT onto the substrate in direct dipping method without any additional patterning process. Generally, in previous researches, many other groups formed the self-assembled monolayer on the whole substrate by totally depositing some surface treatment materials such as aminopropyltriethoxysilane (APTES) or PLL to enhance the attachment of SWCNTs [4-6]. However, the wholly deposited self-assembled monolayer makes the SWCNTs to be totally attached onto the wafer so that additional patterning processes must be needed to eliminate the uncecessary current path through SWCNT outside the channel region. In the self-patterning technique, however, by patterning the surface treatment materials (PLL) with inkjet-printing technology at the region where we wanted to draw in the process step of surface treatment, semiconducting SWCNTs were only attached at the PLL-patterned region without any additional processes. Furthermore, to utilize the self-patterning technology for fabricating the TFT device, I optimized various printing conditions and pattern sizes of PLL, and their effects to the fabricated TFT were also investigated. And based on this technique, high-throughput self-patterned SWCNT TFTs array (72 devices) was successfully implemented on the 2 cm square Si/SiO_2 substrate, and these will be discussed in this chapter.

3.2. Experimental methods

3.2.1. Fabrication Process

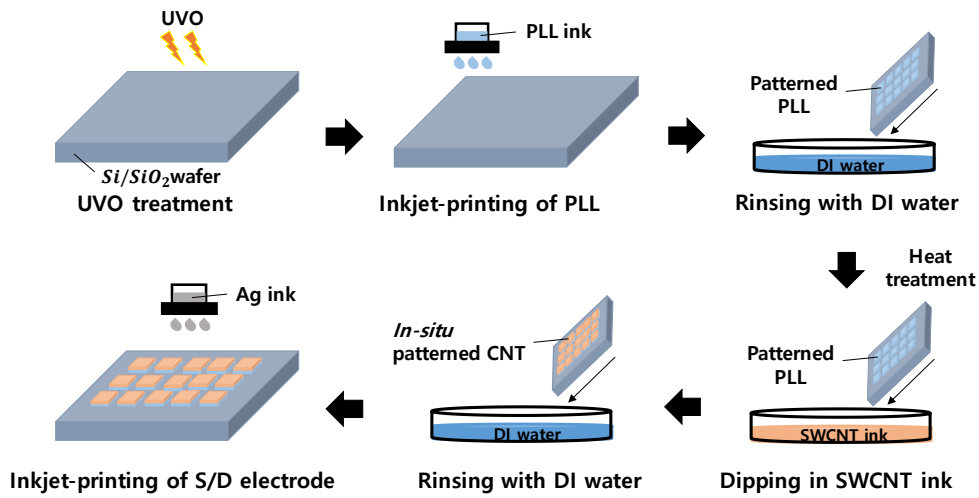

Figure 3.1. Overall fabrication process of SWCNT TFT with inkjet-printing of PLL technique.

Figure 3.1 shows the overall fabrication process of SWCNT TFTs with the inkjet-printing of PLL technique. For printing the PLL, drop-on-demand piezoelectric type inkjet-printer was used in this chapter, which is mentioned in chapter 2. And the substrate and its cleaning procedure are also the same as chapter 2. The prepared substrate was exposed with UVO lamp in chamber to form hydroxyl group on its surface. In this case, the optimized treatment time of UVO is different from the one from the previous chapter, because the deposition aspect of the inkjet-printed PLL film was slightly different from that of the wholly-dipped PLL film. So, the treatment time was set to 5 minutes. Then, the PLL material,

which helps the attachment of SWCNT, was inkjet-printed onto the target substrate and sustained for 5 minutes. After that, I sequentially rinsed the substrate with DI water, blew with N_2-gun, and dried with hot plate at 110 ˚C for 10 minutes to remove the unwanted residue of PLL. In the treatment process, the important thing is the optimization of various parameters, which are the printing conditions of inkjet-printing and pattern size of PLL, for the inkjet-printing of PLL due to fabricating fully-optimized PLL film on the substrate and normally-operated TFT device, and these will be discussed in next section. After the treatment process, the PLL-patterned substrate was immersed into semiconducting SWCNT ink, rinsed with DI water for one minute, and blown with N_2-gun. For the SWCNT ink in this chapter, the acid-added SWCNT ink was used because I can observe the phenomenon of successful patterning with inkjet-printing of PLL technique much faster than the case of as-purchased SWCNT ink based on the conventional dipping method [7]. Utilization of the multi-dipping technique for the self-patterning technique will be discussed in next chapter 4. On the SWCNT layer, source and drain electrodes were inkjet-printed with piezoelectric type inkjet-printer by using metal-organic based silver, and the substrate was sintered with hot-plate at 130 ˚C for 30 minutes. Formation method of source/drain electrodes mentioned above is also the same as chapter 2.

3.2.2. Measurement Details

The SWCNTs inside the channel area were analyzed with scanning electron microscope (SEM) equipment (S-4800, HITACHI Ltd.). And the optical

images were obtained with optical microscope (DSX510, Olympus Corp.) and digital camera in inkjet-printer device (Dimatix-2831, Dimatix Corp.). Electrical characteristics of the SWCNT TFTs such as transfer and output curves were measured with agilent 4155C semiconducting parameter analyzer.

3.3. Results and Discussions

3.3.1. Optimization of printing conditions of PLL

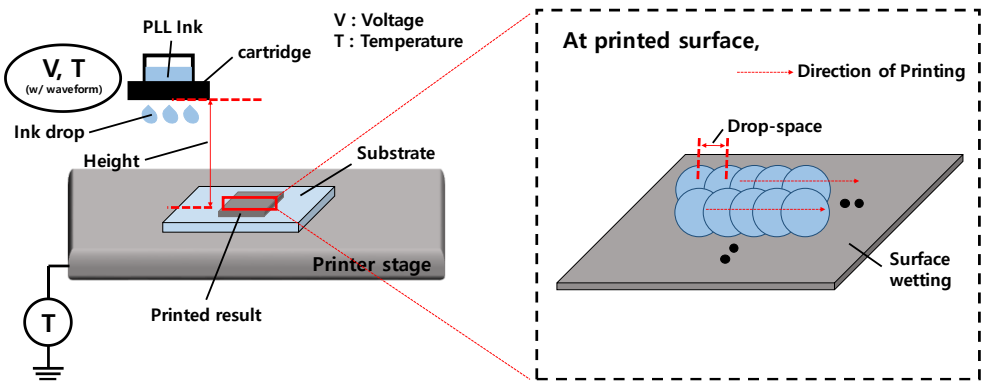

Figure 3.2. Optimization parameters of printing conditions of PLL based on piezoelectric type inkjet printing system.

In piezoelectric type inkjet-printing system, wetting conditions of substrate, jetting conditions (nozzle voltage, waveform, etc.) from nozzle which control the shape and velocity of ink drop, cartridge height, temperature of printer plate which control the evaporation speed of dispersed ink, and drop-space of ink are needed to be optimized to clearly form the patterned PLL layer onto the target substrate (Figure 3.2). If not, some residues still remain after the surface treatment process, resulting in the degradation of TFT performance and the wetting issue after following processes. Results of patterned PLL fabricated with un-optimized conditions are shown in figure 3.3. Therefore, fully optimized printing conditions of PLL must be utilized to reduce these unwanted residues on the substrate after finishing the patterning process of PLL.

First of all, conditions related with the stable jetting (waveform, nozzle

voltage, nozzle temperature) were optimized because stable ink jetting is the most basic component of inkjet-printing technology. Then, the other conditions related with stain-free patterning of the PLL were optimized. Among them, printing temperature and drop-space are the key parameters to fabricate the stain-free PLL pattern. When simply investigating the effect of printing temperature without changing and optimizing any other conditions, as the printing temperature increased, not only did the amount of the residues and stain of PLL increase after finishing the treatment process due to fast evaporation of the ink at the substrate, but also the nozzle was easily clogged during printing (Figure 3.4). Therefore, the temperature of printer plate was set to room temperature (R.T.).

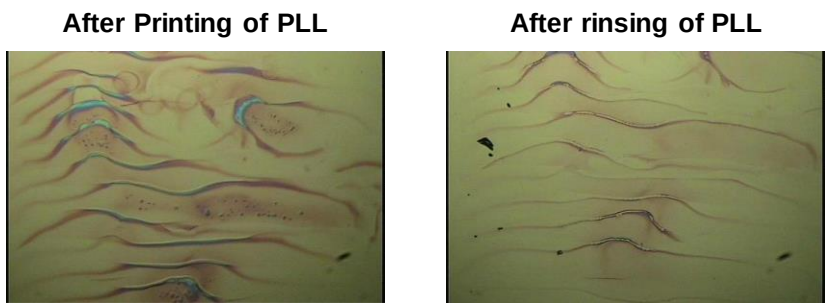

Figure 3.3. Optical images of inkjet-printed PLL in case of un-optimized printing condition.

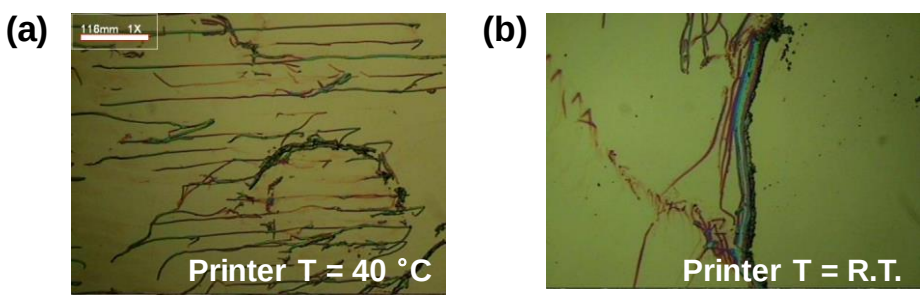

Figure 3.4. Optical images of inkjet-printed PLL in case of the printer temperature of (a) 40 °C and (b) R.T. (Other conditions are the same and un-optimized.)

After setting the jetting and temperature condition, drop-space of PLL ink was controlled. The definition of drop-space is the distance between each ink drop (distance between the centers of two neighboring drops) as described in figure 3.2. Specifically in PLL ink, as shown in figure 3.5, the closer the drop-space was, the more stains and coffee-rings the substrate had. Moreover, if the drop-space was very far, the pattern exhibited discontinuous plane, resulting in non-uniform amine-functionalization of the printed pattern. Therefore, considering the results from figure 3.4 and 3.5, there should be an optimum printing temperature and drop-space value for depositing the PLL with the inkjet-printing, and I set the drop-space of 55 ~ 60 μm with the temperature of R.T. for the optimized printing.

Overall, for fabricating the TFT device with the inkjet-printing of PLL technique, optimization of printing condition of PLL should be needed to eliminate the residues at the substrate after finishing the treatment process of PLL, and almost all residues and stains were successfully removed when utilizing my fully-optimized printing conditions of PLL (Figure 3.6).

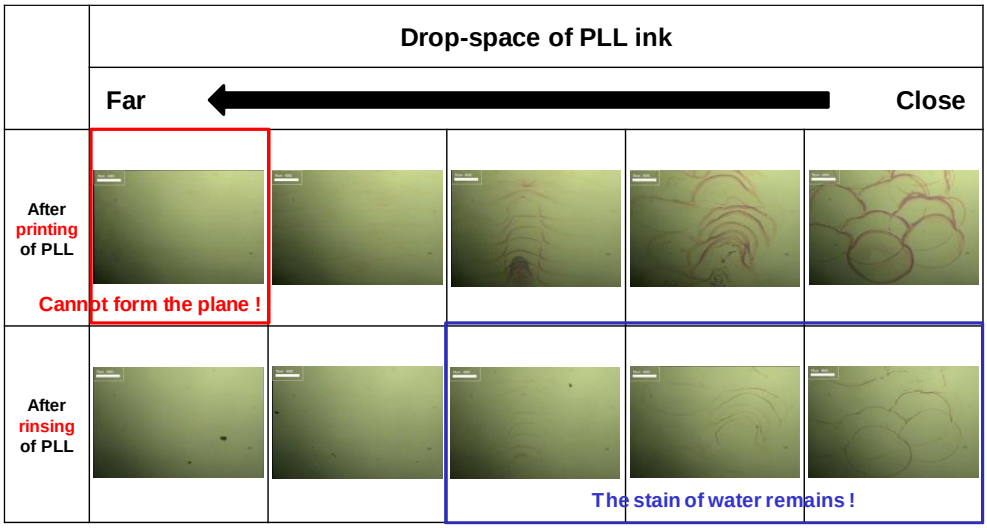

Figure 3.5. The effect of drop-space for the formation of patterned PLL.

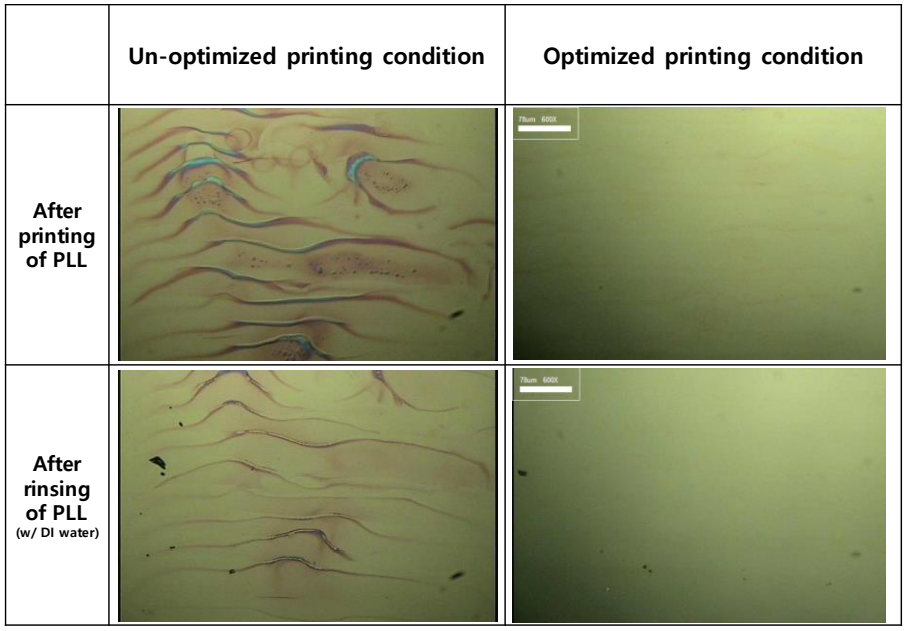

Figure 3.6. Comparison of optical images of inkjet-printed PLL in case of (a) un-optimized and (b) optimized printing condition.

3.3.2. SEM Analysis of Successful Patterning of SWCNT

To check the ability to *in-situ* pattern the semiconducting SWCNT only at the PLL printed region, pre-PLL-patterned substrate was dipped into the SWCNT ink, and SEM images were obtained at the PLL non-patterned region (region A) and patterned region (region B) from the substrate. In figure 3.7, although the substrate was wholly dipped in the SWCNT ink, many semiconducting SWCNTs were only attached at the PLL patterned region (region B) while the SWCNTs were not observed at the PLL non-patterned region (region A). This result clearly shows that semiconducting SWCNTs is only attached at the printed region of PLL where we want to deposit them when applying this self-patterning technique. In other words, successful *in-situ* self-patterning of SWCNT based on the direct dipping method can be possible with the developed technique without any additional patterning process.

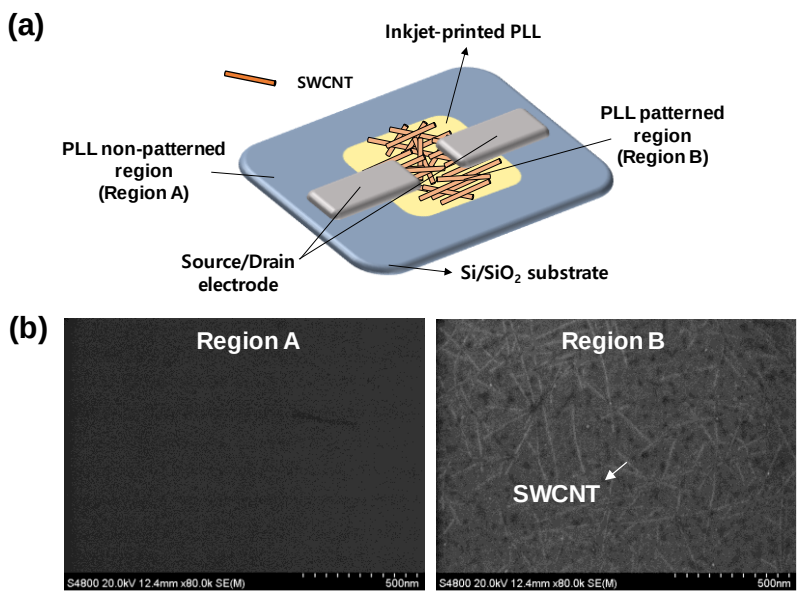

Figure 3.7. (a) Schematic image and (b) SEM images of PLL non-patterned region (Region A) and PLL patterned region (Region B) in the same substrate.

3.3.3. Electrical Characteristics

For further investigating the self-patterning effect of semiconducting SWCNT for the TFT device, two substrates were prepared and compared by investigating the electrical performance of fabricated TFTs (Figure 3.8a). Based on the direct dipping method of SWCNT, one is to attach the SWCNTs onto the substrate where the PLL was wholly deposited by dipping method (device (a)), and the other is to attach the SWCNTs onto the substrate where the PLL was inkjet-printed (device (b)). PLL was not patterned and the device was not physically isolated after the deposition of SWCNT in case of device (a), however, PLL was patterned and its pattern size was set to 1 mm x 1 mm square in case of device (b). Channel length (L) and width (W) of the channel area of TFTs were 135 μm and 180 μm, respectively. Gate voltage (V_{GS}) was swept from 5 V to -5 V (forward sweep of p-type transistor) and the drain current (I_D) was measured at the drain voltage (V_{DS}) of -1 V. When referring to the transfer and output characteristics, in device (a), transistor was not normally turned-off at the off-region because of the high gate leakage current caused by unwanted current path through un-patterned SWCNTs outside the channel area and the edge of the substrate. On the other hand, PLL patterned device (device (b)) was normally turned-off and it exhibited proper transistor characteristics compared with the former one, which is the mobility of 2.76 cm^2/Vs, log(on/off current ratio) of 3.6, and turn-on voltage of 4.1 V (Figure 3.8b and 3.8c). It means unnecessary leakage current path through dispensable SWCNTs outside the channel region is significantly reduced by *in-situ* patterning the SWCNT with the self-patterning technique, and this result is consistent with the result of SEM analysis as described in previous chapter 3.3.2.

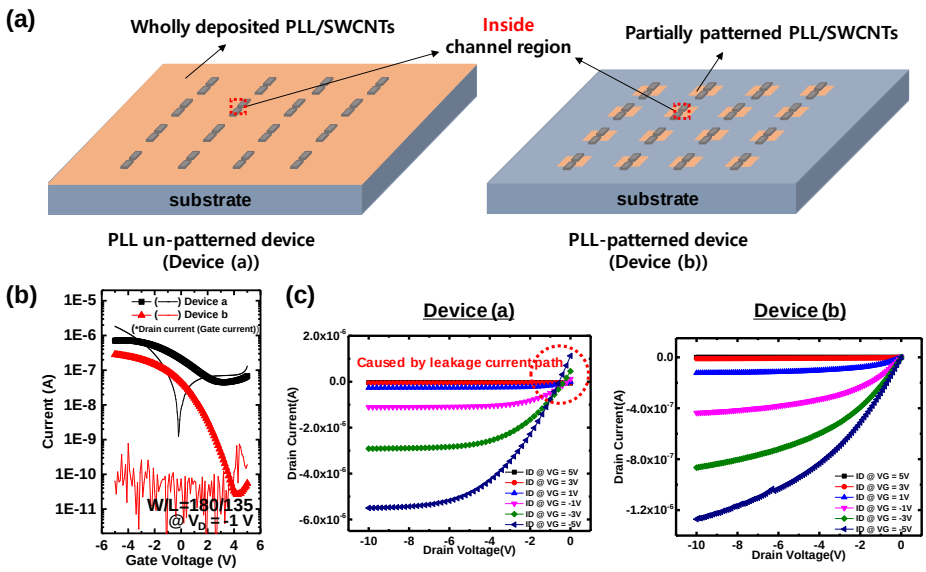

Figure 3.8. (a) Illustration of PLL un-patterned (device (a)) and PLL patterned device (device (b)). Comparison of (b) Transfer and (c) output characteristics between device (a) and device (b).

Consequently, printing the surface treatment material, especially the PLL, with fully-optimized conditions before depositing the SWCNTs can enable the high-quality semiconducting SWCNTs to be selectively attached at the region where we want to be patterned on the substrate, resulting in proper operation of fabricated TFT devices.

3.3.4. Two Main Parameters for Inkjet-printing of PLL

3.3.4.1 Effect of Water-satin of PLL

In chapter 3.3.1, I optimized the various conditions for eliminating the water-stain of PLL inside the channel region. Generally, in TFT, the residues inside the channel negatively affect the electrical performance of the device due to these following reasons: (i) these can act as a pollutant and defect in the active region, (ii) these can cause higher surface roughness and wetting issues after the following processes such as the deposition of source/drain electrode. Therefore, it can be possible to degrade the electrical characteristics of device from them [8,9]. To experimentally verify the effect of water-stain, I extremely decreased the drop-space of PLL ink (~ 5 μm) to increase the amount of stains after the treatment process (Figure 3.9a) and checked the electrical characteristics of the fabricated TFT. In case of the un-optimized one, it exhibited metallic electrical performance (not turned-off), although it exhibited the on-current level of 200 nA, which is much lower density of SWCNTs than the device fabricated with the optimized printing condition in figure 3.8b. This is because the unnecessary current path are occurred from the remained water-stain inside the channel. And moreover, at the outer-boundary of PLL-patterned region, the issue of water-stain is more serious compared with the optimized one (Figure 3.9b). For these reasons, unwanted residues of PLL inside the channel region, which can degrade the electrical performance of TFT and wetting property after following processes, must be eliminated with the fully optimized conditions.

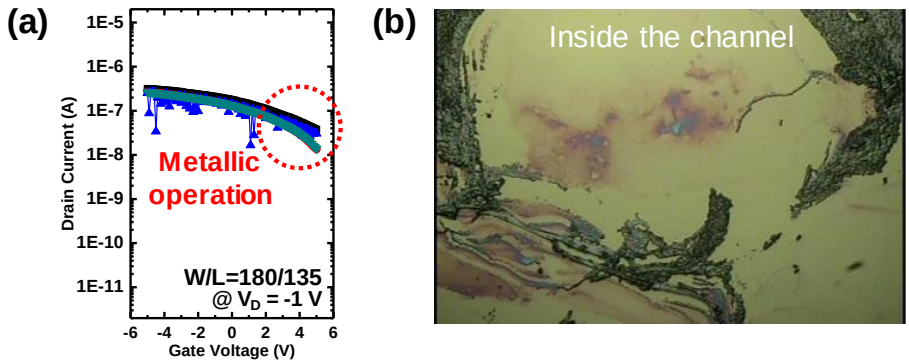

Figure 3.9. (a) Transfer characteristics and (b) optical image inside the channel region of device fabricated with extremely un-optimized condition of drop-space.

3.3.4.2 Effect of Pattern Size of PLL

Based on the results from chapter 3.3.3, unnecessary leakage current path through unpatterned SWCNT was significantly reduced by the *in-situ* patterning of SWCNT with the inkjet-printing of PLL technique. So, to further investigate the relationship between the the pattern size of PLL and the electrical performance of TFT device, I fabricated three types of TFT device with different pattern sizes of PLL (500 μm, 300 μm, 150 μm square) on one substrate and compared the electrical characteristics of each case. In this section, the channel length (L) and width (W) of the channel area of TFTs were 135 μm and 145 μm, respectively. Gate voltage (V_{GS}) was swept from 10 V to -5 V (forward sweep of p-type transistor) and the drain current (I_D) was measured at the drain voltage (V_{DS}) of -1 V. Figure 3.10a shows the representative transfer characteristics from each pattern size, which has very similar on-current level in three cases, and figure 3.10b shows

the measured results of the fabricated TFTs. Based on the electrical characteristics, although the average values of mobility and turn-on voltage exhibited almost similar in all cases, the on/off current ratio of the device, especially the off-current characteristic, was improved as the pattern size of PLL was reduced. It means that the current path at the off-state of the device from the unnecessary SWCNT outside the channel is dramatically reduced in the pattern size of 150 μm, even though the density of SWCNTs, which affects the on-current level of the device, is almost the same in three cases [10]. All extracted electrical characteristics from figure 3.10 are summarized in table 3.1.

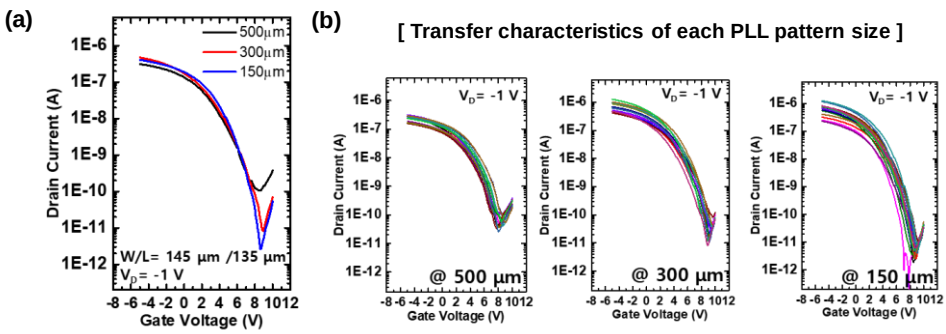

Figure 3.10. Transfer characteristics of (a) data set of similar on-current level in each case, (b) measured TFTs devices of three different kinds of PLL pattern size.

Parameter	PLL pattern size		
	500 μm square	300 μm square	150 μm square
Mobility [cm^2/Vs]	**2.56 ± 0.96**	**2.75 ± 1.12**	**2.89 ± 0.87**
Turn-on Voltage [V]	**7.70 ± 1.07**	**8.54 ± 0.43**	**8.64 ± 0.55**
Log(on/off current ratio)	**3.82 ± 0.25**	**4.65 ± 0.16**	**4.92 ± 0.25**
Off-current level [A] (average current level)	**196 p**	**71.6 p**	**8.85 p**

Table 3.1. Extracted parameters from transfer characteristics in figure 3.10b.

To additionally verify this concept, I fabricated un-patterned TFT device as described in figure 3.8a (device (a) in figure 3.8) and physically isolated it with two isolation methods about the same channel, which are rough isolation and harsh isolation as expressed in figure 3.11a. When measuring the electrical characteristics of aforementioned two cases, the harsher isolation of channel region is, the smaller off-current level of the device is (figure 3.11b). It also means that the leakage current path through unnecessary SWCNTs decreases when reducing the pattern size of the active layer, assuming the pattern size is larger than the channel dimension (figure 3.11c).

Overall, if the printing size of PLL decreases, the device performance, especially off-current properties, can be significantly enhanced, and moreover, it can be possible to apply these phenomenon to implement the minimized and highly integrated electronic applications.

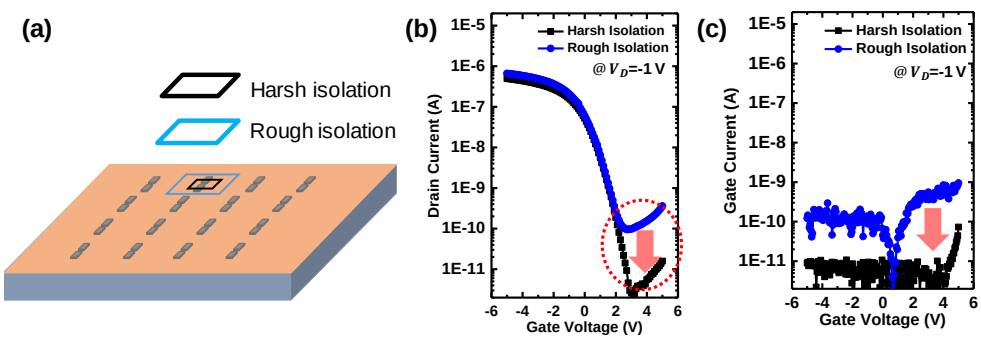

Figure 3.11. (a) Illustration of harsh and rough isolation method of un-patterned device. (b) Transfer characteristics and (c) gate leakage current (different device set from the case of (b)) of each isolation method.

3.3.5. Array Implementation

Finally, based on the newly-developed self-patterning technique of semiconducting SWCNT by printing the PLL, I implemented SWCNT TFTs array (72 devices) on 2 cm square Si/SiO_2 substrate with the optimized printing conditions and the pattern size of 150 μm. Figure 3.12a shows the transfer characteristics of all transistors at array, and fig. 3.12b ~ 3.12d are the statistical distributions of electrical characteristics of the array. Yielding ratio of the array was over 98%, and it exhibited the average value of μ of 2.68 cm^2/Vs, $V_{turn\text{-}on}$ of 3.98V and log(on/off current ratio) of 4.92. Furthermore, not only the water-stain of PLL inside the channel but also the leakage current path through unwanted SWCNT region was not found at all at the array fabricated with the fully-optimized conditions. Therefore, based on the array's characteristics, I can conclude that the developed self-patterning technique can enable the successful implementation of high-throughput and high-performance SWCNT TFTs array based on the direct dipping method of SWCNT without any time-consuming fabrication process. Furthermore, this technique can be utilized for implementation and commercialization of flexible/stretchable electronic applications based on large-area SWCNT TFTs array in the future.

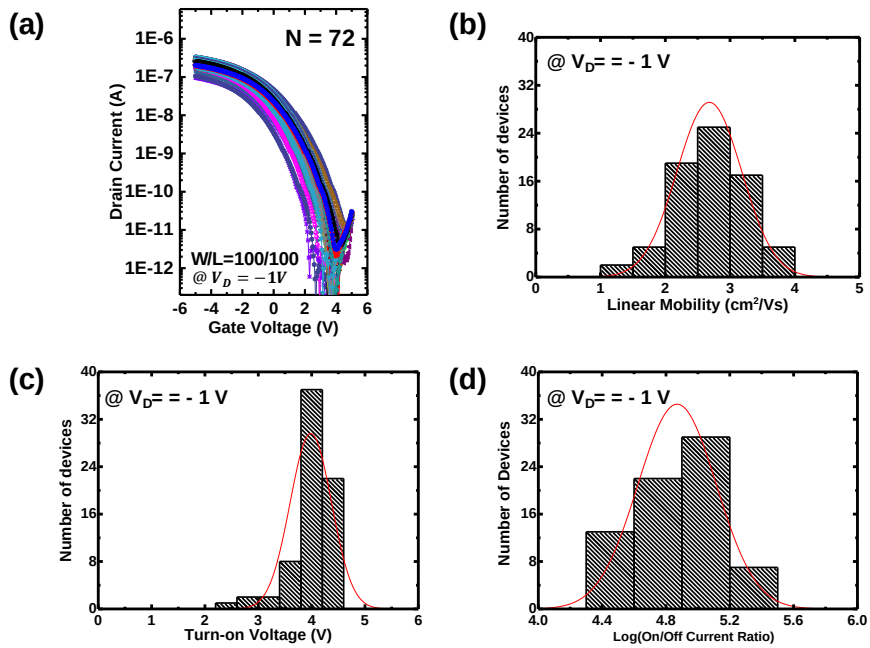

Figure 3.12. (a) Overall transfer characteristics and (b), (c), (d) Statistical distributions of electrical characteristics extracted from the SWCNT TFTs array.

3.4. Chapter Summary

In this chapter, *in-situ* patterning method of semiconducting SWCNT was implemented, which is called “self-patterning technology”, to simply fabricate the SWCNT TFT with the direct dipping method by inkjet-printing the surface-treatment material that enhances the attachment of SWCNT. With the optimization of the printing conditions and the printing size of PLL pattern, not only were the residues inside the channel which degrade the TFT performance significantly eliminated, but also the leakage current level caused from unnecessary SWCNT decreased. And based on this technique, I successfully implemented high-throughput SWCNT TFTs array of 72 devices on the Si/SiO_2 substrate. I believe this technique could provide a guideline for implementing R2R fabrication with high-throughput and high-performance SWCNT array in advanced large-area electronic applications such as active matrix for sensor and display.

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Chapter 4

Fast and Self-patterning Technique of Semiconducting SWCNT for High-throughput and High-resolution Solution-processed TFT

4.1. Introduction

In previous two chapters, I implemented “multi-dipping technique” and “inkjet-printing of PLL technique (self-patterning technique)” to overcome the main issues of direct dipping method. Multi-dipping technique can reduce the overall process time by more than half and improve the electrical characteristics of SWCNT TFTs at the same time. And inkjet-printing of PLL technique can enable the simultaneous patterning of SWCNT during the dipping process without any additional patterning process. Herein, I attempted to integrate these two techniques for fabricating the SWCNT TFT device and verified the feasibility and applicability of the integrated technique for the implementation of high-throughput and high-resolution SWCNT TFT with the direct dipping method. Based on the

core advantages of each technique, I defined the integrated technique as “fast and self-patterning technique”. Specifically in this chapter, verification process of the applicability of this technique based on the two criteria, which are the large-area scalability and micro-patternability, is introduced. The meaning of large-area scalability is to verify the possibility of implementing the high-throughput and high-performance TFTs array for large-area electronic applications, and that of micro-patternability is to verify the possibility of implementing the micro-patterned TFT device for high-resolution electronic applications.

In this chapter 4 of my dissertation, the large-area scalability was verified by implementing 8 x 8 SWCNT TFTs array on the 2 cm square Si/SiO_2 substrate with the fast and self-patterning technique. With investigating and examining the array’s characteristics such as yielding ratio, electrical characteristics and their statistical distributions, I successfully reconfirmed the core advantages of my integrated technique. Moreover, the micro-patternability was verified by demonstrating all-electrohydrodynamic (EHD)-printed SWCNT TFT with the integrated one on the glass substrate. The reason for newly introducing the EHD printing technique in this chapter is to effectively implement high-resolution-patterned SWCNT TFT with remarkable micro-patternability of EHD printing. In particular, by fully engineering the jetting and printing condition of all layers of TFTs in the EHD printing, I successfully implemented low-temperature processable and high-performance all-EHD-printed SWCNT TFT, and the advantages of the integrated technique were also successfully emphasized. Concept of this chapter 4 is summarized in figure 4.1.

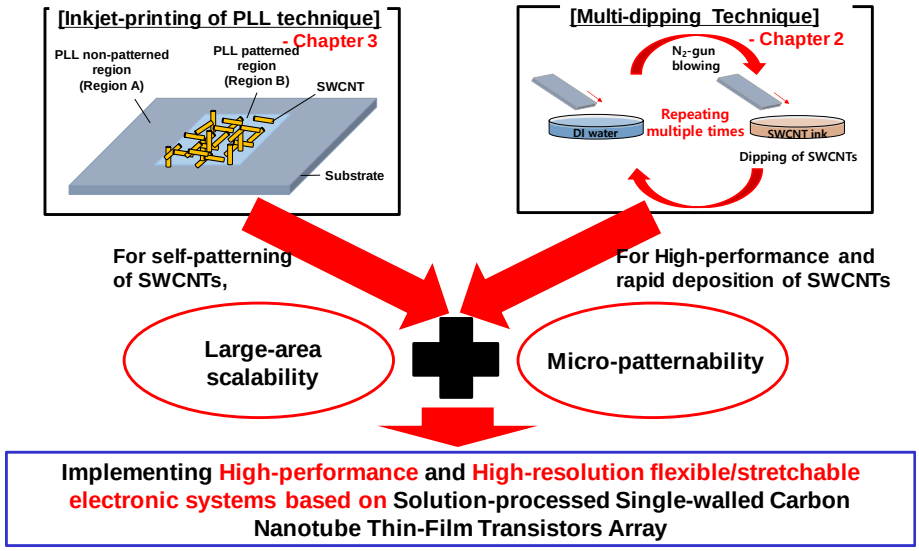

Figure 4.1. Concept of the work performed in chapter 4 of this dissertation.

4.2. Verifying Large-area Scalability of Two Techniques for Implementing SWCNT TFTs array

4.2.1. Fabrication Process

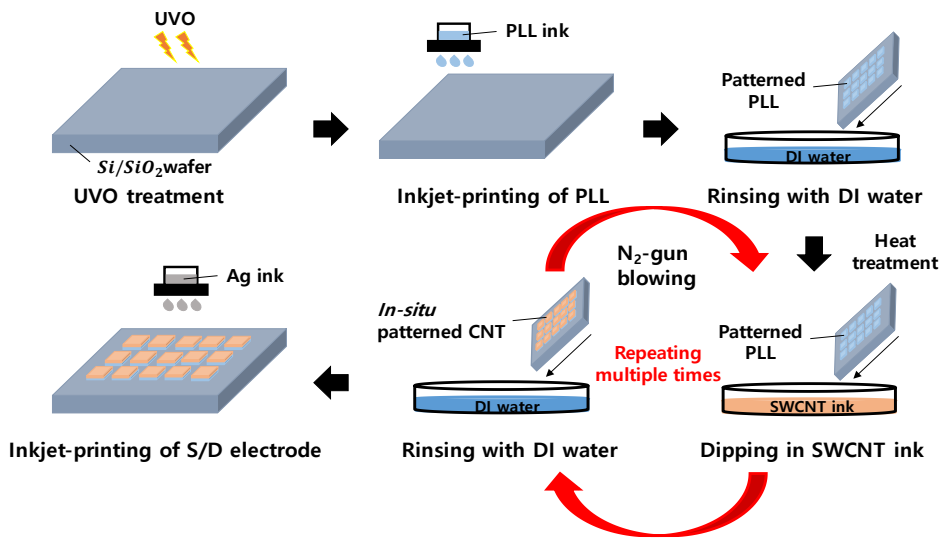

Figure 4.2. Overall fabrication process of 8 x 8 SWCNT TFTs array on 2 cm Si/SiO_2 substrate with fast and self-patterning technique.

Figure 4.2 shows the overall fabrication process of 8 x 8 SWCNT TFTs array on 2 cm Si/SiO_2 substrate for the verification of large-area scalability. Overall process and used materials were the same as previous chapters. Different things are that the PLL was simply inkjet-printed on the substrate only at the desired region, and this pre-PLL-patterned substrate was multi-dipped into the SWCNT ink. For implementing the array, 8 x 8 PLL matrix was inkjet-printed onto UVO-treated substrate, then the substrate was sequentially rinsed with DI water, blown with N_2-

gun, and dried with hot plate to remove the unwanted residues of PLL. The pattern size of PLL was set to 200 μm square, and the distance between each PLL was set to 2 mm. On the matrix of PLL, multi-dipping was performed with the SWCNT ink, and unit-dipping time was slightly changed for efficient deposition of SWCNTs. In this case, the acid-added SWCNT ink was used because I could effectively compare the results with the fabricated array in previous chapter 3 that was fabricated with conventional one-time dipping method of acid-added SWCNT ink. In particular, the throughput and electrical characteristics of each array (the case of applying the multi-dipping versus the case of applying the one-time dipping) were compared, and these will be discussed in next chapter 4.2.2. Length (L) and width (W) of the channel were 120 μm and 140 μm, respectively.

4.2.2. Electrical Characteristics

Figure 4.3a shows measured transfer characteristics of all TFTs in array, and figure 4.3b and 4.3c are the hysteresis and output characteristic of unit device in array, respectively. Yielding ratio of the array was 95.31%, and the array exhibited the average value of μ of 6.01 cm^2/Vs, log(on/off current ratio) of 5.25, $V_{turn-on}$ of 3.74 V, and S.S. of 0.48 V/dec (Figure 4.3d). In hysteresis characteristic (Figure 4.3b), the value of hysteresis voltage was measured at half of on-current level between forward and reverse sweep, and device exhibited the value of 0.4 V. Generally, as the hysteresis phenomenon of pristine SWCNT TFT on oxide surface is derived from the defects and the hydroxyl groups that can act as charge traps, existence of the hysteresis at the fabricated device is reasonable, and it is consistent

with the previous related study of SWCNT TFT. By the way, the value of hysteresis voltage in case of the device fabricated with fast and self-patterning technique is almost the same as that of the device fabricated with conventional one-time dipping method or developed multi-dipping method (Figure 2.6 in chapter 2). Because of the identical TFT structure with the same dielectric layer when comparing all cases, I can insist that my newly-developed fast and self-patterning technique does not negatively affect the hysteresis characteristics of fabricated TFT [1]. In addition to these device electrical characteristics, there is no contact issue between active layer and source/drain electrode when applying the integrated technique, considering the output characteristic (Figure 4.3c). Overall, these results suggest that it is possible to effectively implement the high-performance and high-throughput SWCNT TFTs array based on the integration of newly-desired two techniques much faster and easier without any degradations of the electrical performance.

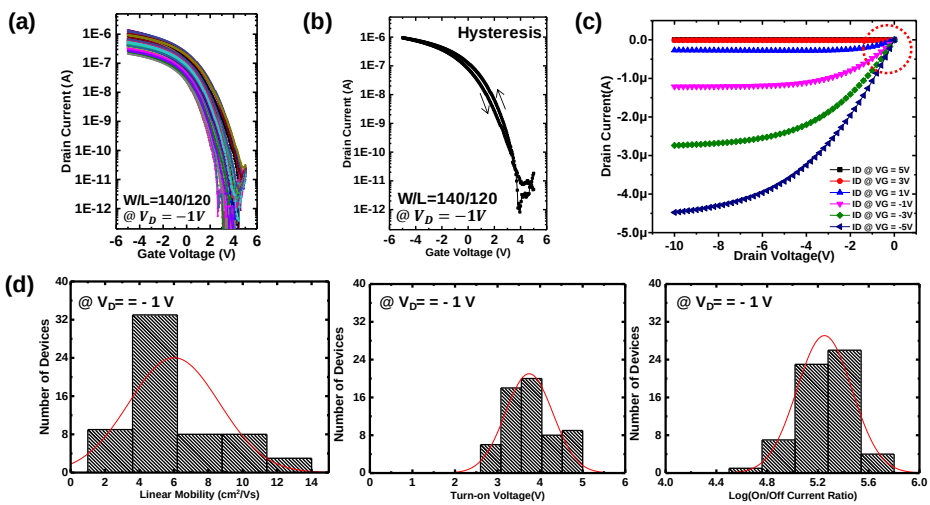

Figure 4.3. (a) Overall transfer characteristics of measured TFTs in array. (b) Hysteresis and (c) output characteristic of unit device in SWCNT TFTs array. (d) Statistical distribution data of electrical characteristics extracted from transfer characteristics in figure 4.3a.

For more detailed analysis, two arrays fabricated with two different dipping methods of SWCNT, which are conventional one-time dipping technique (fabricated in chapter 3) and multi-dipping technique (fabricated in this chapter), were compared with considering the throughput and electrical characteristics of each array. In this section, let me call the array from the multi-dipping technique on PLL-printed substrate array-A, the array from the one-time dipping technique on PLL-printed substrate array-B. The statistical distributions of electrical characteristics of each array are summarized in figure 4.4. In array-A, all electrical characteristics of array were enhanced from the point of views of mobility, on/off current ratio, turn-on voltage, and subthreshold swing in comparison with those extracted from array-B. In other words, much higher electrical performances can be obtained when applying the multi-dipping technique on the pre-PLL-patterned substrate for implementing the SWCNT TFTs array, and the advantages of multi-dipping technique as mentioned in chapter 2 are still maintained for the self-patterning technique. By the way, the variation of device characteristics existed in both array-A and array-B. The as-purchased 95%-semiconducting SWCNT ink used in my work contains 5 % of metallic impurities in the ink, so that the randomly deposited metallic impurities can be existed at the randomly formed SWCNT network fabricated by direct dipping method. Furthermore, the degree of aggregation of SWCNTs inside the channel also affect the variations of it. Therefore, these deviations could be decreased with more highly-purified semiconducting SWCNT ink over 99.9% or some newly-developed alignment methods of SWCNT network based on the direct dipping method [2,3].

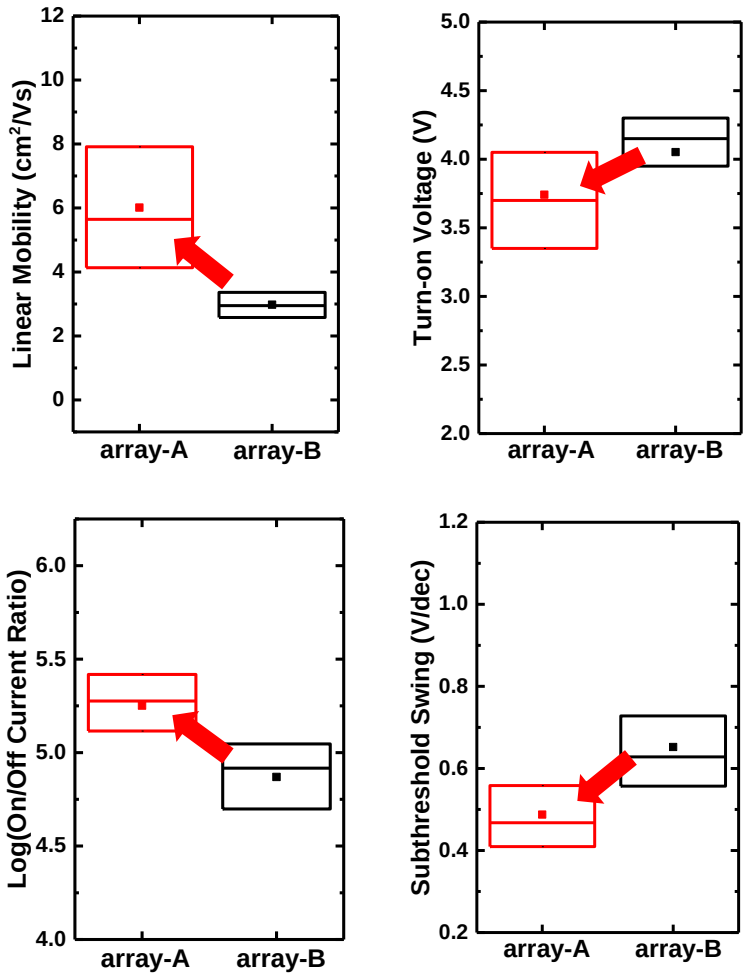

Figure 4.4. Statistical distributions extracted from electrical characteristics and their comparison between array-A and array-B.

4.2.3. Sub-chapter Summary

In this sub-chapter 4.2, high-performance and high-throughput 8 x 8 SWCNT TFTs array was successfully implemented on 2 cm square Si/SiO_2 wafer with the integration of “multi-dipping” and “inkjet-printing of PLL” techniques. Based on the characteristics of array, the advantages of the multi-dipping techniques mentioned in chapter 2 were also maintained at the *in-situ* patterned SWCNT network. Moreover, when considering the off-current level of the fabricated array, the small and self-patterned semiconducting SWCNT network was successfully obtained with the fully-optimized printing conditions mentioned in chapter 3 without any unwanted residues and additional patterning process. And, the fabrication throughput of the array was still very high (> 95%) with the integrated technique, though each device was apart from 2 mm distance onto the 2 cm square substrate. It means that the developed fast and self-patterning technique can also maintain the advantages of direct dipping method, such as high yield ratio over the large-area and low process complexity. Overall, these results suggest that I successfully verified the possibility of implementing high-performance SWCNT TFTs array with high fabrication yield ratio for the large-area electronic applications. Lastly, I can summarize this sub-chapter with 5 keywords as follows: “Low-temperature processable”, “Fast and self-patterned”, “Large-area scalable”, “High-performance”, “High-throughput” solution-processed SWCNT TFTs array.

4.3. Verifying Micro-patternability of Two Techniques for Implementing SWCNT TFTs array

4.3.1. Concept of High-resolution and EHD Printing Technique

Nowadays, one of the key components for the development of future display industry is to satisfy the demand for high-resolution. For example, although the resolution of display for smartphone requires at least 500 pixel per inch (ppi) for commercialization, the one for more realistic display, such as virtual reality (VR) or augmented reality (AR) display, requires at least 5000 ppi to be utilized in real life [4-7]. Therefore, the development of high-resolution can make humans' life more comfortable because it can be possible to obtain the clear and real view image (Figure 4.5).

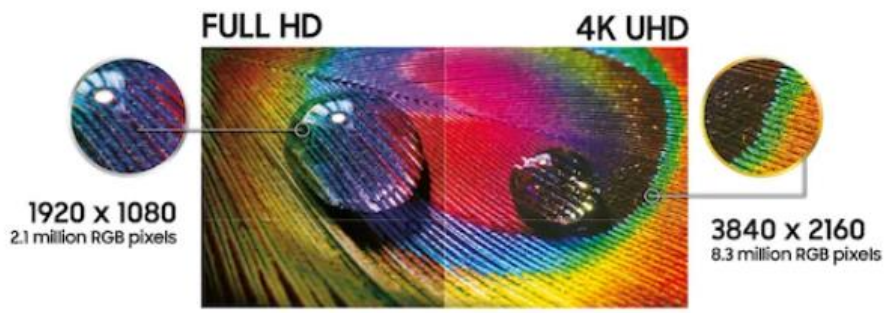

Figure 4.5. Concept of high resolution display implemented by Samsung Display Corporation (Source : Samsung Display).

In this regard, various patterning technologies for implementing ultrafine pixel have been widely used such as piezoelectric type inkjet-printing technology and transfer printing. However, there are some limitations for utilizing these techniques, such as limited printing scale about tens of micrometer in case of piezoelectric type inkjet-printing or difficult scalability in case of transfer printing, to fabricate the high-resolution devices [8]. To solve these limitations in this chapter, I adopted the electrohydrodymanic (EHD) printing technique to effectively verify the micro-patternability of my device. EHD printing technique is jetting the ink by controlling the electric field between the nozzle and the printing substrate. In EHD printing, by optimizing the various jetting conditions like nozzle bias and frequency, a meniscus at nozzle tip is changed to the shape of Taylor cone, resulting in much clearer and smaller pattern size that exhibits the scale of a few micrometer onto the substrate. Furthermore, with these advantages, the EHD printing technique could easily deposit the ultrafine high-resolution patterns based on the solution-process, which consequently facilitates the implementation of micro-patterned and high-resolution electronic devices. So, many related researches have been previously performed from stretchable electrode for various applications to pixel device such as display panel (OLED) or neuromorphic device (Figure 4.6) [8-11]. In this chapter 4.3, I also chose the EHD printing technique to verify the micro-patternability of the developed “fast and self-patterning technology” with implementing the high-resolution patterned all-EHD-printed SWCNT TFT.

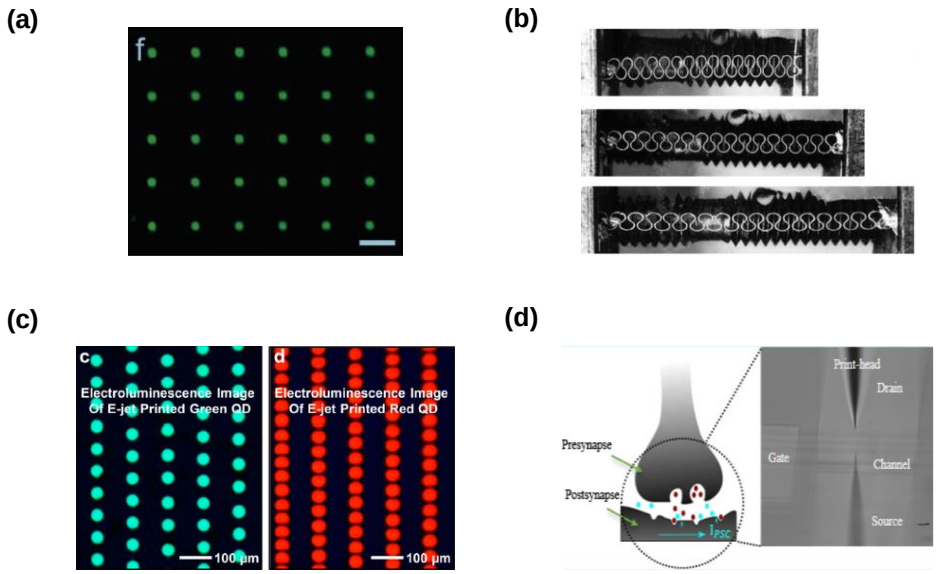

Figure 4.6. Previous researches about EHD-printed device applications (Source : (a) small molecule OLED [8], (b) self-healable electrode [9], (c) quantum dot (QD) [10], (d) neuromorphic [11]).

4.3.2. Optimization of Each Layer of TFTs with EHD printing

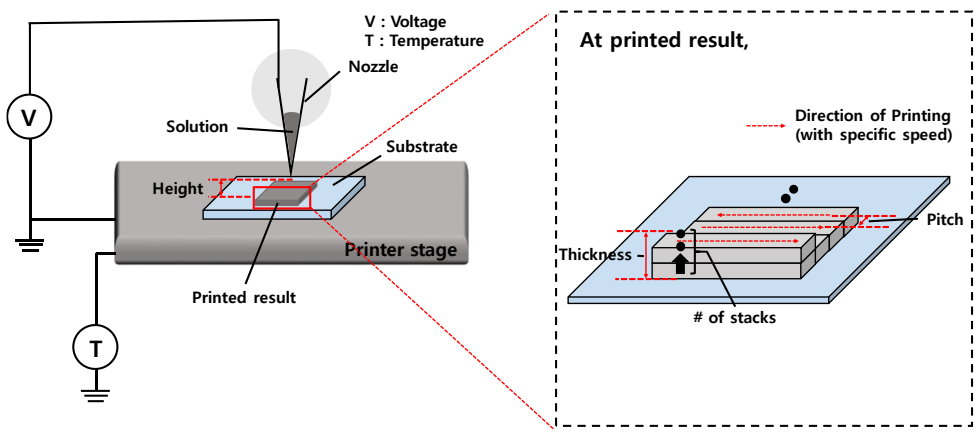

Figure 4.7. Principle and various parameters for EHD printing technique.

To optimize the printing conditions of EHD, there are many parameters to successfully form the desired fine-pattern. In my strategy, these can be divided into two main categories, which are (i) stable ink jetting from the nozzle and (ii) optimized surface property and design fitted with the used ink (Figure 4.7).

(i) Stable jetting from the nozzle

Firstly, an ink-type material for printing and a size of nozzle (large, standard, or superfine) are needed to be selected. Various characteristics of the solvents like viscosity, boiling temperature, and vapor pressure are important factors to stably eject the ink from the nozzle, and the nozzle size should also be carefully chosen based on the prepared ink. For example, although the superfine nozzle can eject very small amount of ink drop because of small aperture size of nozzle (about 1 μm), highly viscous or evaporative ink is not easily ejected with it. After finishing the selection of printing materials, various parameters (voltage waveform, amplitude, frequency, nozzle height, etc.) controlling the electric field between the nozzle and the stage are needed to be engineered for deforming the meniscus of the ink at the nozzle tip for stable and sharp jetting. With un-optimized jetting conditions, for example, sprayed or non-uniform pattern could be obtained due to formation of the inappropriate meniscus for the jetting at the nozzle tip. Therefore, stable jetting from the nozzle by controlling the various aforementioned parameters is one of the most important factors to fabricate the desired pattern.

(ii) **Optimized surface property and design fitted with the ink**

With stable jetting conditions, consideration of the wetting property and related design structure on the target substrate should be needed to be considered

for forming the well-defined pattern. If I want to change the wetting property of the substrate for the well-defined pattern, some surface treatments with various materials are needed before the printing. And, to form high-quality thin-film layer on the prepared substrate, which is fitted well according to the intended purpose of the usage, various characteristics of film, such as surface roughness and thickness, should be fully optimized by controlling the design parameters. In my strategy for the category (ii), there are two main fabrication steps to achieve it. First of all, very thin-film layer is formed onto the substrate by printing the multiple lines with some design parameters such as pitch (distance between each single line) and printing parameters such as printing speed and cut-off voltage. Then, this printing step is iterated certain times for desirable performance. Only in this case, I can consequently obtain the high-quality thin-film of desired pattern whose design factor and performance can be easily controlled and optimized.

Overall, by combining the two strategies mentioned in (i) and (ii), I successfully optimized the printing conditions based on the EHD printing technology.

In this regard, to implement the all-EHD-printed SWCNT TFT device for verifying the micro-patternability of my technique, printing conditions for each layer of TFT should be optimized to obtain high-performance TFT. Generally, the most basic form of TFT consists of electrode (gate, source, drain), dielectric (insulation layer), and active (semiconducting) layer. Accordingly, various technical issues for printing the each TFT layer are existed and needed to be considered for the implementation of all-EHD-printed SWCNT TFT (Figure 4.8). For example, electrical resistance and channel dimension should be considered to

print the electrode, and the capacitance value with certain thickness and insulating property should be considered to print the dielectric layer. In particular, as the deposition of active layer is based on the integration of the multi-dipping and self-patterning technique, related printing conditions of PLL should be also optimized as mentioned in the previous chapter 3.

In this chapter 4.3.2, I briefly introduce the optimized results of each layer of TFT based on the EHD printing technology. For implementing the device, glass substrate (Eagle-XG, Freemtech corp.) was used as the substrate, and nanoparticle-based Ag (DGP 40LT-15C from Advanced Nano Products Corp.), poly(4-vinylphenol) (PVP, Sigma-aldrich Corp.), and semiconducting SWCNT were used as the electrode, dielectric, and active material, respectively. To sharply define each layer, electrode and dielectric layer were printed at the printing temperature of 30 °C with superfine nozzle. And referring to the chapter 3, PLL was printed at the temperature of R.T with superfine nozzle not to make the unnecessary residue of PLL. After printing, all layers were annealed in hot plate with different ramping conditions, and maximum annealing temperature of the fabrication process is 160 °C.

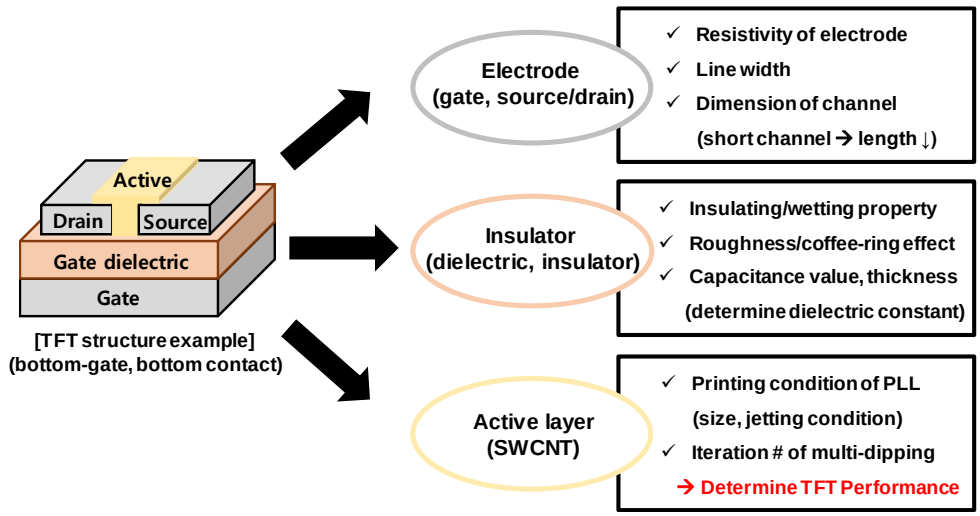

Figure 4.8. Considered technical issues for implementation of all-EHD-printed SWCNT TFT.

4.3.2.1. Electrode

Figure 4.9a shows the optical and SEM image of optimized electrode line, and figure 4.9b shows the current-voltage curve of it. Among the various parameters for printing, designed line width and the number of stacking are the key parameters to determine the electrical conductivity of metal electrode. If the number of stacking decreased for the same width and length of electrode, the resistance value increased (about 100 ohm) because the network of Ag nanoparticle became sparse. And the conductivity of the electrode was degraded when reducing the line width under 4 μm, even though the number of stacking was above 10 times (Figure 4.9c and 4.9d). Overall, adequate line width and its corresponding number of stacks are needed to form the optimized electrode, and I set the electrode line width of 11 μm with 2.6 μm pitch and the stacking number of 3~4 times for the desirable performance with minimized line width based on these results. The

fabricated electrode exhibited the resistance value of 34 ohm at the length of 110 μm and the thickness of 90 nm, resulting in the calculated resistivity value of 1.71 x 10^{-7} ohm·m. Although this value is 10 times higher than the value of bulk Ag, considering the annealing temperature and the previous reported resistivity of the printed thin-film Ag, obtained resistivity of my EHD-printed electrode with fully-optimized condition is reasonable [12,13]. So, I can insist that my desired conditions for printing the electrode are appropriate to fabricate the electrode for the all-EHD-printed SWCNT TFT device.

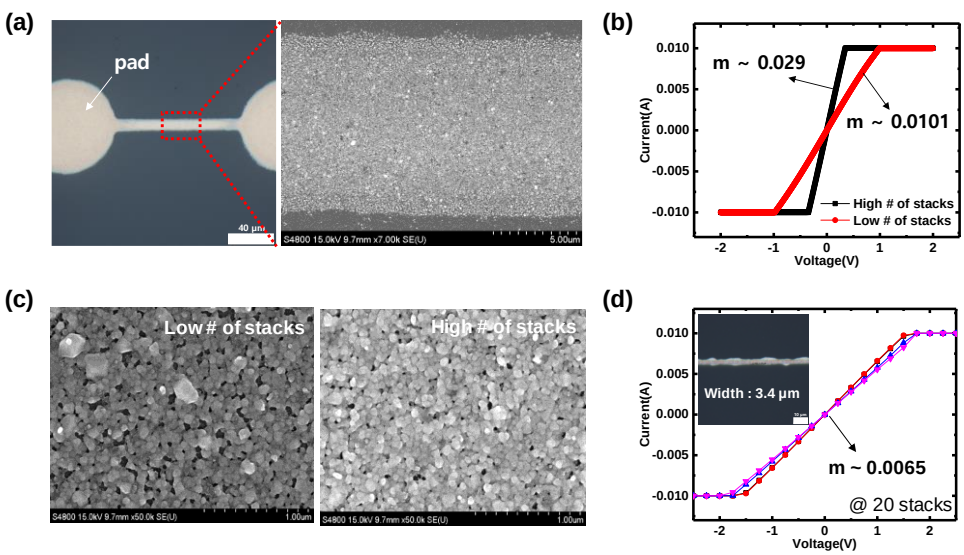

Figure 4.9. (a) Optical and SEM image of EHD-printed electrode line. (b), (c) I-V curve and SEM image of electrode line fabricated with un-optimized (low # of stacks) and optimized (high # of stacks) condition. (d) I-V curve of electrode line fabricated with very narrow width (width of 3.4 μm).

4.3.2.2. Dielectric

To fabricate the high-quality dielectric film, insulating property and surface morphology are need to be considered. Among the various parameters, solvent of PVP, the number of stacking, minimization of voltage for very thin-film single layer, and printing speed are the main factors to determine them. First of all, I used mixed solvent system for dissolving the PVP powder and its cross-linker (poly(melamine-co-formaldehyde), PMFM, Sigma-Aldrich Corp.), which are propylene glycol methyl ether acetate (PGMEA, Sigma-Aldrich Corp.) and ethyl alcohol (ethanol, Sigma-Aldrich Corp.), to eliminate a coffee-ring effect. Generally, critical issue of the inkjet-printed film is the existence of the coffee-ring effect at the edge of the layer, and mix-solvent system is one of many solutions for reducing it by controlling the flow of the liquid drop on the substrate. Because the mixed solvents reduce the evaporation gradient of the printed ink, Marangoni flow increases and it reduces the coffee-ring effect [14]. In my case, also, coffee-ring effect was remarkably eliminated with the two solvents system as shown in figure 4.10a, and utilized volume ratio of two solvents was 1:1. In printing process, the minimized printing voltage with optimized speed (0.35 mm/s) was used to fabricate the very thin-film layer, then it was repeated 2 times, which is for the enhancement of the insulation property and surface roughness at the same time (figure 4.10b). Some higher printing voltages than the optimized one could be possible to utilize for forming the dielectric layer without stacking, however, it is very difficult to control the various properties (thickness, leakage current, roughness) of dielectric compared with my approach. Besides, in my strategy, the number of stacking for printing the PVP layer is also very important parameter. With maintaining the

minimized voltage and related conditions, if the number of stacking decreased to 1 time, the printed PVP film exhibited not only rough surface morphology (RMS value of 5.92 nm in 1 layer printing versus that of 2.64 nm in 2 layers printing) but also low breakdown voltage under 5 V resulting from much lower thickness value compared with 2-layers-stacked PVP layer (thickness of 142 nm in 1 layer printing versus that of 300 nm in 2 layers printing) (Figure 4.10b). Overall, minimized printing voltage for very thin-film layer and its corresponding number of stacks should be needed to form highly engineered PVP dielectric layer, and I set the aforementioned fully-optimized conditions for the desirable performance of PVP layer. Figure 4.10a exhibits the optical image of fully optimized EHD-printed PVP film, and figure 4.10c exhibits the current density-voltage (J-V) and capacitance-frequency (C-f) characteristics of it. The fabricated PVP exhibited leakage current density value of 5.1 nA/cm^2 at the E-field of 1 MV/cm and the capacitance value of 8.2 nF/cm^2 at the thickness of 300 nm, resulting in the calculated dielectric constant value of 2.8. When compared to the previous PVP dielectric from my group, which was fabricated with the piezoelectric-type inkjet-printing, my engineered PVP dielectric exhibited much better insulating properties with no coffee-ring phenomena when considering the thickness and insulation properties [15]. Therefore, all these results including the morphology of the surface clearly show that these adopted conditions for printing the PVP layer are well-optimized and suitable for implementing the all-EHD-printed SWCNT TFT device.

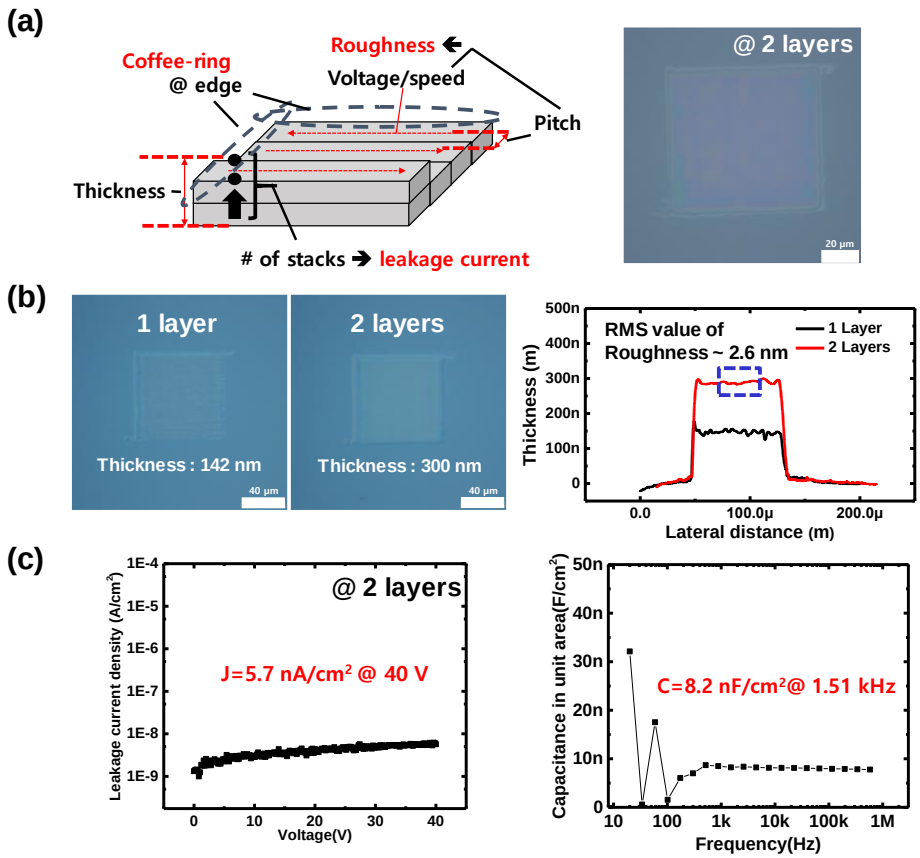

Figure 4.10. (a) Main factors and fabricated results of EHD-printed PVP. (b) Optical images and line profiles of unstacked and stacked PVP. (c) J-V, C-f characteristics of fully optimized EHD-printed PVP.

4.3.2.3. Surface Treatment Materials

Referring to the previous chapter 3, for printing the PLL, optimization of printing conditions of PLL should be needed to eliminate the unwanted PLL residues inside the channel. In case of EHD-printing system, similar to the case of piezoelectric type inkjet-printing, temperature of printer plate, ink condition, wetting conditions of substrate, jetting conditions (nozzle voltage, waveform, etc.) from nozzle, printing speed, and nozzle type are needed to be optimized to form

stain-free PLL pattern onto the target substrate. In this case, however, I used PLL solution of low molecular weight dissolved in DI water (0.01 wt%) for easily and stably jetting the ink with superfine nozzle. And, minimized voltage with optimized speed (0.4 mm/s) was chosen to print the smooth layer of PLL and avoid the unnecessary residue of PLL after the treatment process. The reason why I chose this condition is the same as the one why I chose the specific value of drop-space of PLL for the piezoelectric-type inkjet-printing as mentioned in chapter 3. For example, much lower speed under 0.4 mm/s or much higher voltage than the minimized one increases the residue of PLL inside the channel region, which is the same as the case when the drop-space is reduced. Moreover, very thin-film layer was deposited with the pitch of 2.5 μm that is almost similar value to the width of single-line of PLL printed with above conditions, and it was not stacked. Criteria for those conditions are also based on the aforementioned reasons. With these optimized conditions, I successfully checked that the stain didn't remain inside the channel region after finishing the treatment process. Camera image of EHD jetting of PLL ink and printed result with the fully-optimized conditions are summarized in figure 4.11.

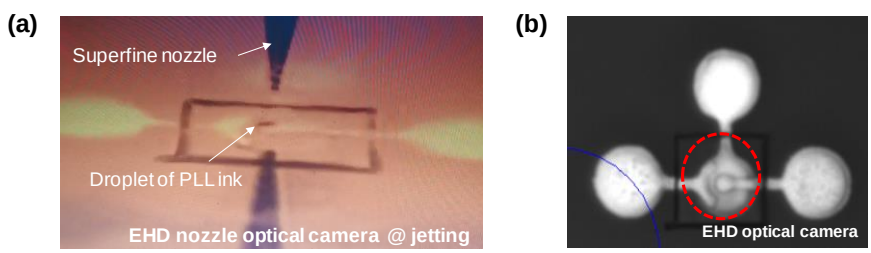

Figure 4.11. Camera image of (a) droplet of PLL ink during jetting and (b) printed result after DI water rinsing.

To further investigate the effect of water-stain in case of EHD-printing, I fabricated the TFT device with the un-optimized printing condition of PLL. As shown in figure 4.12, with the un-optimized printing conditions, the fabricated TFT device exhibited bad contact property (measurement noise) and metallic characteristics (not turned-off) due to the unnecessary current at the off-state resulting from the remained water-stain inside the channel, although it exhibited much smaller density of SWCNTs compared with the other cases when referring to the on-current level (about 52.6 nA). Furthermore, the wetting issues of the following process, which are caused from the residue of PLL, were more serious compared with the optimized one. In figure 4.12b, for example, when the jetting voltage was much higher than the minimized one, printed source/drain electrode, which is to be deposited onto the SWCNT, was disconnected at the outer boundary of printed PLL. This result is also consistent with the investigation of water-stain effect at the piezoelectric type inkjet-printing technique as described in previous chapter 3.

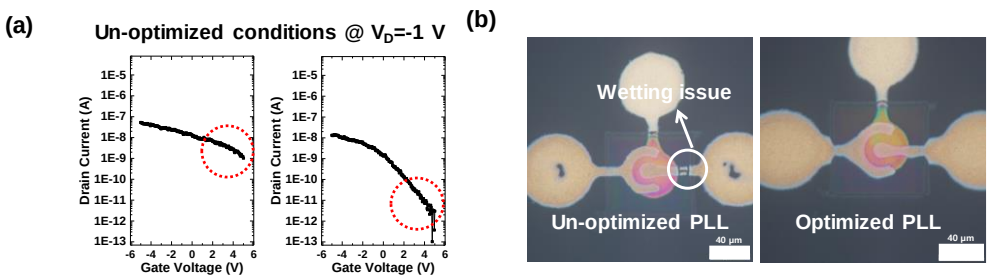

Figure 4.12. Issues at un-optimized printing conditions in all-EHD-printed SWCNT TFT.

After optimizing the printing conditions of PLL, I verified the *in-situ* self-patterning effect of the semiconducting SWCNT with the EHD-printed PLL. Two types of TFT device were prepared, and SEM images at the channel areas were obtained from each device (Figure 4.13). The substrate, which was wholly dipped in PLL, was dipped in the SWCNT ink in case of device (a), while the substrate, which was pre-PLL-patterned by EHD printing, was dipped in the SWCNT ink in case of device (b). Inside the channel, density of semiconducting SWCNTs was much denser in case of device (b) compared with device (a). That means, in case of device (a), although the substrate was wholly dipped in PLL and SWCNT ink, many semiconducting SWCNTs were almost attached onto the surface of silver electrode rather than the channel region. In other words, amine-group was rarely formed inside the channel region with the wholly dipping of PLL due to the difference of wetting property between Ag electrode and PVP dielectric layer. However, deposition mechanism of amine-group is less sensitive to the difference of wetting property of the pre-patterned components of TFT when the PLL is printed, so that the amine-group was properly formed inside the channel region with the EHD-printing of PLL. Overall, the printing technique of PLL, even at the EHD printing, can enable uniform deposition of amine-group onto the channel region regardless of the pre-formed components of the device, resulting in *in-situ* self-patterned semiconducting SWCNT only at the PLL-patterned region, and this result is also consistent with the case of piezoelectric-type inkjet-printing technique as described in previous chapter 3.

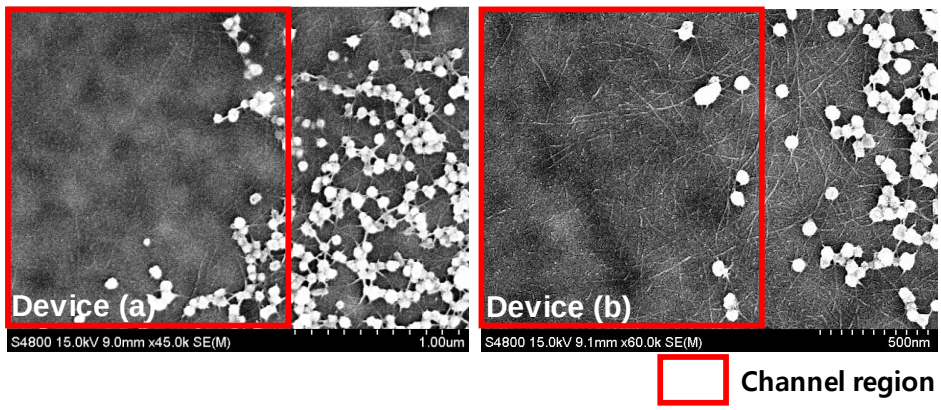

Figure 4.13. SEM images inside the channel region in case of the device fabricated with (a) wholly dipping of PLL (un-patterned PLL) and (b) EHD printing of PLL.

4.3.3. All-EHD-printed SWCNT TFT with Two Techniques

4.3.3.1. Fabrication Process

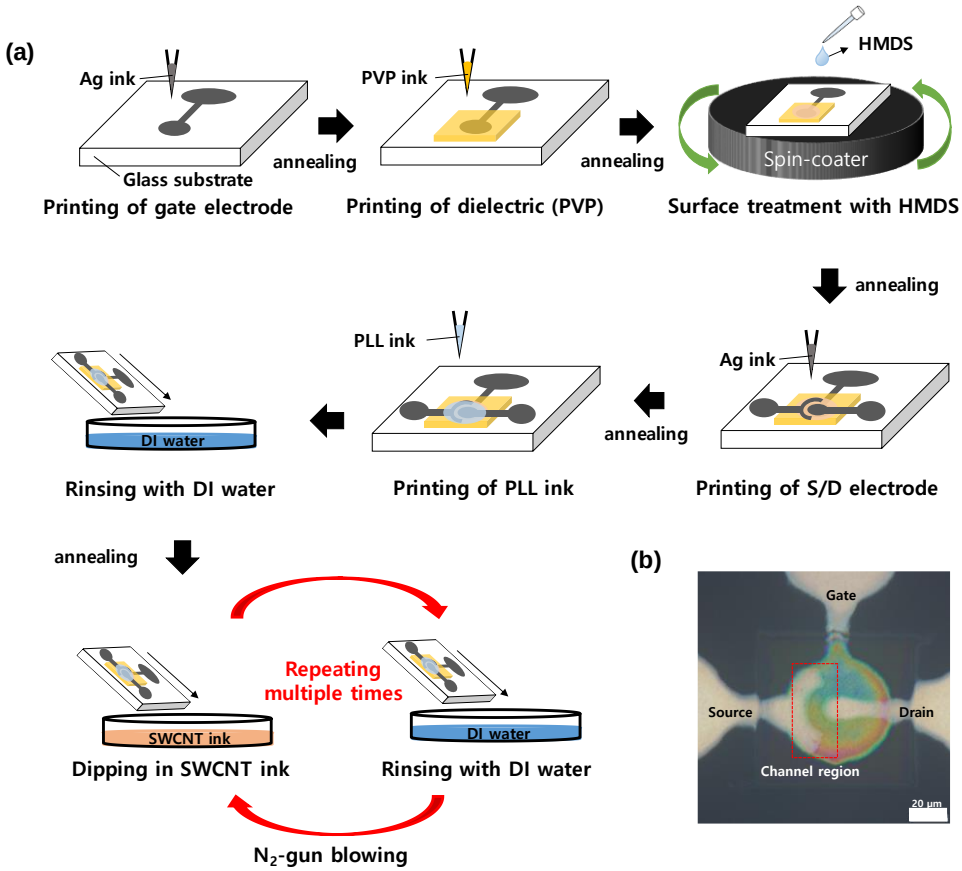

Figure 4.14. (a) Overall fabrication process and (b) optical image of all-EHD-printed SWCNT TFT.

Figure 4.14a shows the overall fabrication process of all-EHD-printed SWCNT TFT. Fully-optimized conditions mentioned in previous chapter 4.3.2 were used to print all the layers of TFT. Before fabrication, the substrate was cleaned with conventional sulfuric acid peroxide (SPM) cleaning (mixture of sulfuric acid and hydrogen peroxide water with the ratio of 4:1) to remove the

adhesive component of the tape and remained pollutants on the as-purchased glass substrate, and it was sequentially rinsed with DI water, acetone, and IPA. Ag ink was printed onto the prepared substrate as a bottom gate whose size was the electrode line width of about 10 μm and the gate diameter of about 57.8 μm, and it was sintered at the maximum temperature of 160 ˚C with ramped condition. Then, the PVP dielectric was printed as a gate dielectric and sintered at the maximum temperature of 160 ˚C with ramped condition. The size of PVP determines the total pixel size of the TFT device and its value was set under 90 μm square. To effectively define the source and drain electrode of the device, hexamethyldisilazane (HMDS) was spin-coated at 3000 rpm for 1 minute to suppress the spreads of top electrode at the PVP surface by changing the surface energy of printed PVP to more hydrophobic, and it was sintered at temperature of 150 ˚C. Onto the HMDS-treated surface, Ag ink was printed as a top source/drain electrode, and its length (L) and width (W) of the channel were 5 μm and 24.74 μm, respectively. After finishing the deposition of top source/drain electrode, I applied the fast and self-patterning technology to form the active layer of the TFT. PLL was printed on the target area with the size of 20-μm-radius half circle, then the substrate was sequentially rinsed with DI water, blown with N_2-gun, and dried with hot plate to remove the unwanted residues of PLL. This pre-PLL-patterned substrate was multi-dipped into the as-purchased SWCNT ink after the surface treatment process. In this case, as-purchased SWCNT ink was used to prevent the bundle effect of the acid-added SWCNT ink that can create the critical degradation at my short channel device whose length is similar scale with the length of nanotube, and I adopted slightly different unit-dipping time for the efficient deposition of given as-purchased SWCNT ink. TFTs with the bottom gate and

bottom contact structure were formed, and the optical image of fully-EHD-printed TFT is shown in figure 4.14b.

4.3.3.2. Electrical Characteristics

Figure 4.15a shows measured transfer characteristics of fabricated TFT, and figure 4.15b and 4.15c are the hysteresis and output characteristic of device, respectively. The device exhibited value of μ of 5.10 cm^2/Vs, log(on/off current ratio) of 5.57, $V_{turn-on}$ of 4.00 V, , and S.S. of 0.33 V/dec. And moreover, the leakage current level of the device is under 2 pA at the measured gate leakage current and the off-current level of the device. In particular, The fusion of highly reduced pattern size of PLL with the EHD-printing technique, the advantages of multi-dipping technique, and high insulating property of high-quality PVP dielectric film enhances the electrical characteristics of the fabricated device, especially at the on/off characteristics and the off-current level, which can ultimately improve the performance of circuit or system based on the SWCNT TFTs such as low-power consumption at the off-state of the device. In hysteresis characteristic (Figure 4.15b), the value of hysteresis voltage was measured at half of on-current level between forward and reverse sweep, and device exhibited the value of 0.25 V. And, in addition to these device electrical characteristic, there was no contact issue between active layer and source/drain electrode by checking the output characteristic, even though all layers of TFT were printed with EHD printing technology and the active layer was fabricated with the fast and self-patterning technique for the micro-patterned TFT (Figure 4.15c). Overall, high-quality thin-

films of each layer of TFT and TFT devices combined with them were successfully obtained with my fully-optimized EHD-printing condition and the integrated technique. Consequently, micro-patterned high-performance SWCNT TFT can be implemented with the integration of newly-desired two techniques much faster and easier way.

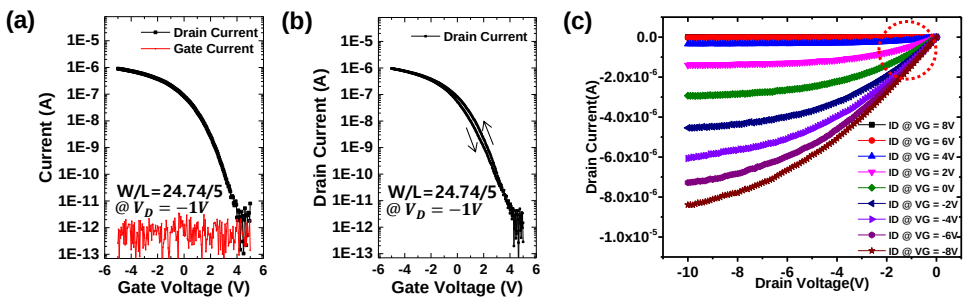

Figure 4.15. (a) Transfer, (b) hysteresis, (c) output characteristics of all-EHD-printed SWCNT TFT device.

4.3.4. Sub-chapter Summary

In this sub-chapter 4.3, micro-patterned SWCNT TFT was successfully demonstrated with the EHD printing technique, which exhibited the total size of tens of micrometer, with the integration of “multi-dipping” and “self-patterning” techniques and fully-optimized printing conditions of EHD-printing technique. With the fully-optimized conditions, processable minimum size of EHD-printed line was under 4 μm, and feature size of manufactured device was under 90 μm square with very small leakage current level under 2 pA based on high-quality EHD-printed dielectric. When compared to the various previous researches related with EHD-printed TFT, my device exhibits remarkable feature size and electrical characteristics of each layer of TFT and itself, such as good conductivity of electrode, very low leakage current level of dielectric and device, proper mobility and on/off current ratio of device at the low operation voltage. Among them, the most remarkable thing is my device can be fabricated at the maximum temperature of 160 °C, which ultimately presents the low-temperature processability of solution-processed SWCNT and my newly-designed “fast and self-patterning technology”. The aforementioned comparisons between my device and related previous researches are summarized in table 4.1 [16-20]. Therefore, I can conclude that I successfully verified the micro-patternability of SWCNT TFTs by applying the EHD-printing technique with the fully-optimized condition and the fast and self-patterning technique to meet the demand for high-resolution electronic applications with the device miniaturization. Lastly, I can summarize this sub-chapter with 5 keywords as follows: “All-EHD-printed”, “Low-temperature processable”, “Fast and self-patterned”, “High-resolution patterned (micro-

patternable)”, “Highly engineered (such as contact property and leakage current)” solution-processed SWCNT TFT with EHD-printing technique.

Table 4.1. Comparison of fabrication and performance of this work with other EHD-printed TFT [16-19].

Previous EHD-printing based TFT	This work	J-U. Park et. al, 2007[16]	T. Sekitani et. al, 2008[17]	Y. Jeong et. al, 2016[18]	Y. Liang et. al, 2019[19]
EHD-printed layer	**All layers** (Ag, PVP, PLL)	Etch resist only	S/D only (Ag)	S/D only (MWCNT/PSS)	All layers (ITO, In2O3, Al_2O_3)
Active material	SWCNT	SWCNT	Organic (pentacene, $F_{16}CuPc$)	Organic (pentacene)	Oxide (In_2O_3 or IGZO)
Active Deposition/patterning method	**Dipping Self-patterning**	CVD grown, dry-transfer Reactive ion etching	Vacuum Shadow masking	Organic molecular beam system	Printing of In_2O_3
Feature size of device	Line width = 3.4 ~ 12 μm **Device size < 90 x 90 μm²**	-	Min. line width = 2 μm (uniformity guarantee)	Line width < 140 μm	Line width = 2 μm
Channel dimension (W, L)	W = 24.74 μm L = 4 ~ 5 μm	W = 70 μm L = 1 ~ 42 μm	W = 300 μm L = 1 ~ 100 μm	W = 3000 μm L = 50 ~ 150 μm	W = 120 μm L = 7 ~ 12 μm
Maximum process temp. (°C)	**160**	-	~ 150	120 <	**350**
Operating voltage (V)	VG : -5 V ~ 5 V VD : -1 V	VG : -20 V ~ 20 V VD : -0.5 V	VG : -3 V ~ 3 V VD : - 2.5 V or 2.5 V	VG : -40 V ~ 10 V VD : - 40 V	VG : -2 V ~ 2 V VD : 2 V
Mobility of device (cm^2/Vs)	5~7	7 ~ 42	0.02 @ $F_{16}CuPc$ 0.3 @ pentacene	0.134 (ps-brush)	117.2 @ In_2O_3 (saturation mode)
Log(on/off current ratio) of device	5.5	1 ~ 3	4 @ $F_{16}CuPc$ 5 @ pentacene	5 ≤	6 <
Leakage current level of device	**< 2 pA**	-	~ 20 pA	~ 20 pA	~ 100 pA
etc.	**- Resistivity of EHD Printed Ag ~ 17 x 10^{-8} ohm·m (@ 90 nm) - Leakage current level ~ 5.1 nA/cm² @ 1 MV/cm (@ 300 nm PVP)**	- Gate – evaporated Cr/Au/Ti - Dielectric – SiO2(CVD), spin-cast - S/D – defined with EHD printed resist layer	- Gate – Evaporated Al - Gate dielectric – AlO_x SAM - Resistivity of EHD Printed Ag ~ 25 x 10^{-8} ohm·m (@ 300 nm)	- Gate – highly n-doped Si - Gate dielectric – thermally grown SiO2	- Sheet resistivity of EHD ITO ~ 4.6 x 10^{-5} ohm·m (@ 10 nm) - Cap. ~ 200 nF/cm² - Leakage current level ~ 1 μA/cm² @ 1 MV/cm (@ 40 nm Al_2O_3)

4.4. Chapter Summary

In this chapter, I attempted to integrate the developed two techniques for fabricating the SWCNT TFT device, which is called “fast and self-patterning technique” in this thesis, and investigated the applicability of the integrated technique for the implementation of high-throughput and high-resolution SWCNT TFT based on the two criteria which are the large-area scalability and micro-patternability. For the verification of large-area scalability, high-throughput and high-performance 8 x 8 SWCNT TFTs array was implemented on the 2 cm square Si/SiO_2 wafer with the integrated technique. And for the verification of micro-patternability, EHD printing technology was adopted to fabricate the high-resolution-patterned thin-film layer, and printing conditions of EHD-printing for the fabrication of TFT including the electrode, dielectric/insulator, and surface treatment materials were fully optimized. Based on the optimized conditions, highly-engineered and high-performance all-EHD-printed SWCNT TFT was successfully demonstrated with the integrated technique on the glass substrate, which exhibited the total size of tens of micrometer and the leakage level under a few pA. Consequently, I can conclude that “Large-area scalability” and “Micro-patternability” of the integrated technique are successfully investigated in this chapter 4, which can ultimately show the feasibility of the fast and self-patterning technique for the implementation of next-generation high-performance and high-resolution flexible/stretchable electronic systems based on the SWCNT TFT.

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Chapter 5

Conclusion

5.1. Summary

In this dissertation, two facile and effective techniques, which are “multi-dipping technique” and “inkjet-printing of surface-treatment material technique (self-patterning technique)”, were developed for resolving the two main issues of direct dipping technique of semiconducting SWCNT to rapidly form and effectively self-pattern the high-quality semiconducting SWCNT layer.

For shortening the deposition time of SWCNT, multi-dipping technique was developed as described in chapter 2. Repetition of DI water rinsing between each dipping step during multi-dipping process make it possible to rapidly deposit the dense and high-quality SWCNT network formation, thus leading to significant reduction in total fabrication time but improved electrical performances for SWCNT TFTs. In addition, deposition mechanism of multi-dipping technique was comprehensively introduced and analyzed with the AFM images of channel region.

For *in-situ* patterning the semiconducting SWCNT without any additional patterning methods, self-patterning technique was developed as described in

chapter 3. Patterning of the surface treatment material, especially the PLL material, with the printing technology enables the SWCNT to be selectively deposited onto the desired region at the target substrate. With the optimization of the printing conditions and the pattern size of PLL, not only were the residues inside the channel which degrade the TFT performance fully eliminated, but also the leakage current level caused from unnecessary SWCNT remarkably decreased, resulting in high performance TFT with the selectively deposited semiconducting SWCNT.

With the integration of two developed techniques, the feasibility and applicability of it for the electronic applications were successfully verified by implementing both centimeter scale of SWCNT TFTs array and tens of micrometer scale of all-EHD-printed SWCNT TFT as described in chapter 4.

All methods used in this dissertation are based on the solution-process whose properties are low-temperature and low-cost processable. In particular, the maximum process temperature for the device fabrication in overall chapters was 160 °C, which can directly show the advantages of solution-process, and I can insist that it can be possible to easily apply the concepts of this dissertation to the flexible/stretchable electronic applications. Moreover, based on the printing technology and its corresponding optimized printing conditions including the piezoelectric-type and EHD-type mentioned in this dissertation, surface treatment materials and other device elements can be precisely patterned as someone desires, which can be helpful to be referred by the engineers who want to fabricate the future advanced circuits and systems.

In summary, storyline of the new developments and in-depth verifications of the two techniques for the solution-processed SWCNT TFTs were introduced in this dissertation. I can summarize this thesis in one sentence as follows: “Effective

solution-processed deposition techniques of semiconducting SWCNT for next-generaiton TFT", and I can additionaly summarize all storylines in another sentence as follows: "Combination of rapid formation technique and *in-situ* selectively-patterning technique for depositing the high-quality semiconducting SWCNTs film based on the direct dipping method and utilization of printed circuit elements with the fully-optimized conditions of inkjet-printing technology". Ultimately, I believe that the high-performance and high-resolution electronic applications based on the SWCNT TFTs array at the flexible/stretchable large-area substrate can be easily and rapidly implemented and commercialized if many research and industry groups refer to this dissertation, resulting in early commercialization and mass production of SWCNT TFTs.

5.2. Limitations and Related Works

5.2.1. Detailed Network Analysis of Multi-dipping Technique

In chapter 2, I demonstrated “multi-dipping technique” and introduced the related mechanism to rapidly deposit the dense and high-quality SWCNT network at the channel region of SWCNT TFT. Based on the electrical characteristics in figure 2.5, it is obvious that the surface density of SWCNTs inside the channel and the on-current level of the TFT device are proportional to the number of iteration in the multi-dipping technique. Generally in SWCNT TFT, rather than optimizing the thickness of SWCNT, SWCNT film density inside the channel region dominantly affects the transistor performances as mentioned in chapter 2 and previous related researches. Device with the proper density of SWCNT (just above the percolation threshold) could exhibit the transistor characteristic. As the density of SWCNT increases, on/off current ratio is decreased, due to the increase of the percolation paths through large amount of the tube-tube junctions. So, to obtain excellent TFT performances, optimization of the density of SWCNT is very important. If the SWCNT films start to be much thicker or much denser than the aforementioned percolation threshold, the on/off characteristics of the SWCNT TFTs could be degraded [1-3]. Therefore, to provide the process reliability to the other engineers who want to utilize the multi-dipping technique, more detailed analysis about the relationship between the surface density of SWCNTs and the number of iteration should be followed. For this reason, I additionally experimented four different iteration numbers in multi-dipping with another as-purchased SWCNT ink (different chemical conditions from the chapter 2) and checked the relationship.

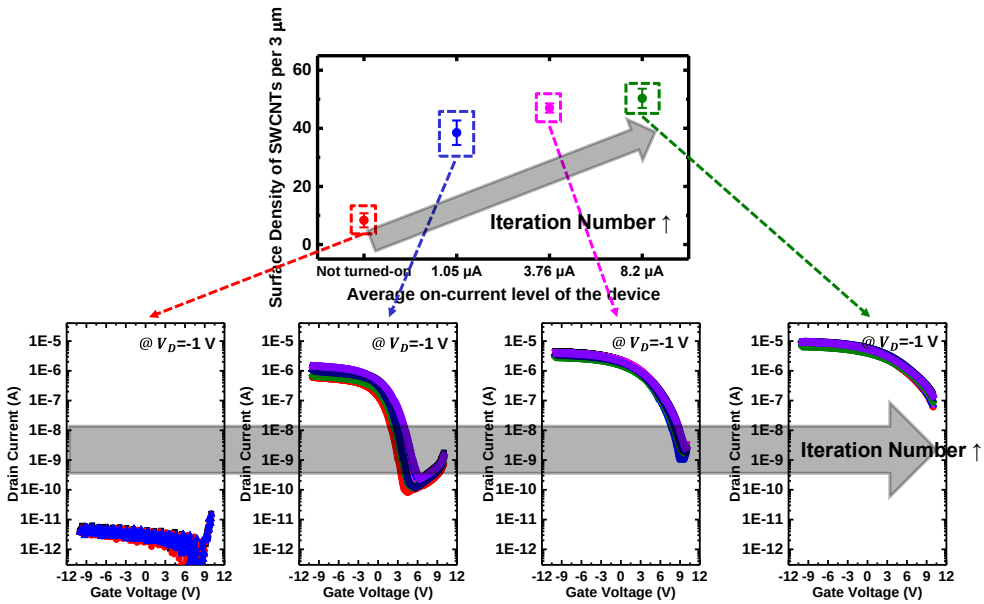

Figure 5.1. Relationship between the surface density of SWCNTs inside the channel and the iteration number in the multi-dipping technique.

The interval of the increase in the number of iteration is the same (5 times increases), except for the 1st case (the case of not turned-on). Gate voltage (V_{GS}) was swept from 10 V to -10 V (forward sweep of p-type transistor) and the drain current (I_D) was measured at the drain voltage (V_{DS}) of -1 V. Figure 5.1 exhibits the relationship between the surface density of SWCNTs and the on-current level of the TFT device for the each iteration time in multi-dipping technique. As the number of iteration increased, surface density of SWCNTs inside the channel area increased, resulting in much higher on-current level of the fabricated SWCNT TFT device. Furthermore, as I mentioned in previous chapter 2 and above, the on/off characteristic of the device was gradually degraded and the threshold voltage and turn-on voltage were positively shifted due to the increase of the percolation paths through the tube-tube junctions between the source and drain electrode. By the way, variation of the density of SWCNT was gradually reduced from the blue-dotted

square to the green-dotted square despite the same increase in the iteration number of multi-dipping. This is because the area for further deposition based on the electrostatic interaction of SWCNT is reduced as the iteration number increases (or the amounts of the attached SWCNTs increase). In other words, the surface density of SWCNTs could be saturated when the iteration number exhibits much higher values.

Considering the general diffusion equation, following three expressions are satisfied:

$$(I)\ \frac{d\rho}{dt} \sim A_1 k_1 + A_2 k_2, \qquad (II)\ A_1 + A_2 = A, \qquad (III)\ \frac{A_1}{A} = \rho$$

, where ρ, k, A, region 1 and region 2 are the density of SWCNT, assumed diffusion rate of each region toward the target substrate, area of the region, pre-CNT-deposited region and non-CNT-deposited region, respectively. By combining all the expressions, following expressions satisfied:

$$\frac{d\rho}{dt} \sim A[(k_1 - k_2)\rho + k_2] \quad \rightarrow \quad \rho \sim B \cdot \exp(k_1 - k_2) \quad (B: \text{constant})$$

When referring to the experiment result from figure 5.1 and the aforementioned diffusion model, the following conditions have to be satisfied:

$$B < 0\ ,\ k_2 > k_1$$

, and this tendency is consistent with the previous related study of SWCNT TFT based on the conventional one-time dipping [4]. Based on the results, it could be inferred that the SWCNTs in the solution are more likely to be attached onto the amine-terminated surface rather than onto the pre-CNT-deposited surface. Accordingly, the saturation of the surface density of SWCNTs are caused by reduction of the number of area for further deposition based on the electrostatic

interaction between the amine group and SWCNTs.

However, the chemical conditions of the as-purchased SWCNT ink, such as the amount of surfactants, were different whenever I purchased the new SWCNT ink. For example, pH of the SWCNT solution used in chapter 2 was 7.34 and that of the solution used in this chapter 5.2.1 was 6.56. Accordingly, the corresponding process conditions were needed to be re-optimized such as the deposition time in one-time dipping or the number of iteration in multi-dipping, and I indirectly observed them by monitoring the pH of the solution and set the iteration time (or range of iteration time) based on it for utilizing the multi-dipping technique. After the optimization, I can observe similar phenomenon and tendency all the time [5]. Therefore, more statistical data set based on the various independent variables (such as pH of the as-purchased SWCNT ink, surface property of the target substrate, etc.) should be needed to be obtained for precisely offering (i) the reference data about the relationship between the surface density of SWCNT and the iteration number in multi-dipping with the on-current level of the fabricated TFT at the various ink conditions and (ii) the more quantified deposition mechanism and related equation modeling (such as diffusion constant) of the multi-dipping with more digitized and visualized image processing program, which ultimately enable the other engineers to further develop and commercialize some real circuit applications based on the developed multi-dipping technique.

5.2.2. Reliability and Encapsulation for All-EHD-printed TFT

In chapter 4.3, I demonstrated all-EHD-printed SWCNT TFT based on the integrated technique ("fast and self-patterning technique") and checked the applicability of the developed technique. However, it is noted that the solution-processed SWCNT TFTs commonly exhibit the bias instability caused from the charge trapping at the dielectric layer such as water/oxygen molecules at the ambient conditions. Considering the real circuit applications, that can deteriorate the reliability and the further commercialization of the electronic devices based on the high-resolution-patterned SWCNT TFT device fabricated with EHD printing technology because the electronic device exhibits different operation whenever or wherever someone uses. Therefore, many researches including my group have adopted some facile methods such as encapsulation with various passivation layers and real-time tuning of the threshold voltage with double-gate structure as shown in figure 5.2 [6-8].

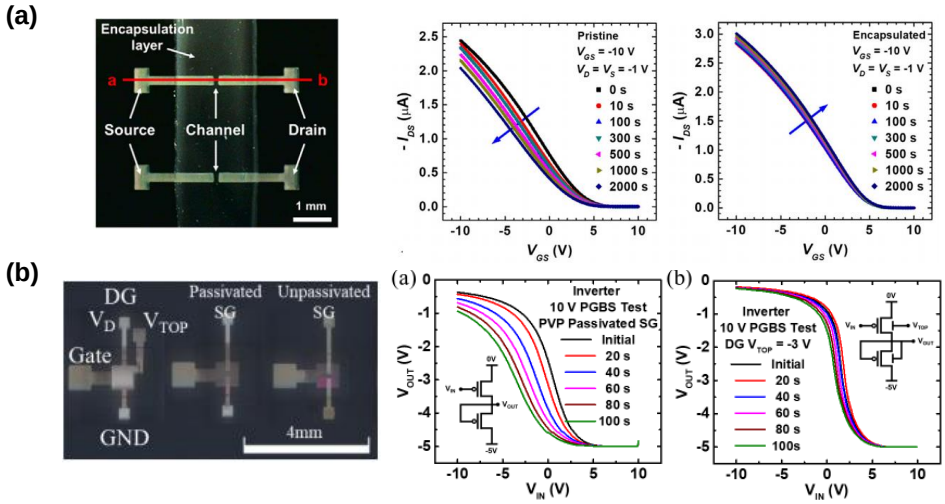

Figure 5.2. Previously reported methods in my group for obtaining the reliability of SWCNT TFTs in case of (a) encapsulation [6] (b) double-gate structure [7].

For the real applications of my developed EHD-printed device, vertically-stacked structure is chosen for the highly-integrated and high-resolution system, so that the whole device is encapsulated with the developed PVP dielectric layer from the oxygen and water molecule in the environment (mentioned in chapter 4.3.2.2, submission in preparation of appendix-[3]). By the way, previously reported paper mentioned that the PVP dielectric could exhibit some hysteresis phenomenon from the slow polarization after the thermal curing process, so the circuits for the real applications with PVP dielectric could exhibit different switching properties [9]. However, PVP dielectric material has great advantages for implementing the all-solution-processed, especially all-EHD-printed, SWCNT TFTs including my research because of low process-complexity, low-temperature processability, low hysteresis characteristic, and mechanically flexibility [7,10,11]. Overall, to effectively show the reliability of the fabricated device, especially the dielectric/insulation layer, it is essential to perform more detailed bias stress tests, such as positive gate bias stress test (PGBS) or the positive/negative bias temperature instability (PBTI, NBTI) under various conditions, and to further consider the facile methods for eliminating these unwanted instability.

5.3. Recommendation for Future Researches

Based on this dissertation, I draw the summary roadmap of solution-processed SWCNT TFT for the researchers and engineers in the field of electrical and display engineering (Figure 5.3). These are divided into 4 steps, and detailed explanations of each step are as follows:

Step 1. Fundamental: Many advantages of solution-processed SWCNT TFT are in the spotlight. So, there are many various deposition methods of semiconducting SWCNT ink, and among them, direct dipping method is the best way to deposit the SWCNTs with its various advantages such as low-cost, high-uniformity and low process-complexity. However, it has some limitations for the mass production and commercialization in the near future.

Step 2. Development: Therefore, core-technologies to resolve them are developed. In this step, investigating the originality, repeatability and feasibility of the developed technique is very important. For example, if the developed process is too difficult to use or too complex to install the fabrication-line (fab-line) system, it is not suitable to commercialize and nobody wants to use that system. In this dissertation, “multi-dipping technique” and “self-patterning technique” are developed with considering these issues, and these techniques are something new, repeatable, and very facile technique for the utilization.

Step 3. Verification: After that, verification for the applicability of developed techniques is very important. In this thesis, I choose the implementation

of large-area and high-resolution electronic applications as the purpose of the usage. Even though I investigate it based on the two criteria, which are the large-area scalability and micro-patternability in the unit device scale at the laboratory, there are many other various criteria for the someone's intended usage. For the commercialization and mass-production, I think the development of equipment for the fab-line production capable of mass production and roll-to-roll system should be preceded, and that is also to be verified based on the criteria according to the purpose of its usage.

Step 4. Application: After completing the technical review, real appplications used in soneone's everyday life should be developed. In the research field of TFT including the SWCNT TFT, implementation of large-area, high-resolution, and flexible/stretchable backplane for the signal-process and performance enhancement with the form of active-matrix is the final goal for the next-generation electronic applications [12-14]. Therefore, commercialized products based on SWCNT TFTs are to be rapidly and efficiently fabricated and provided to the customers based on the developed techniques and equipments. Based on this dissertation, I suggest that circuit applications with the integration of my two techniques, which is "fast and self-patterning technique", be also the one of the possible approaches for the mass production and commercialization of next-generation large-area advanced flexible/stretchable electronic applications such as active matrix backplane for OLED, photodiode, and biosensors.

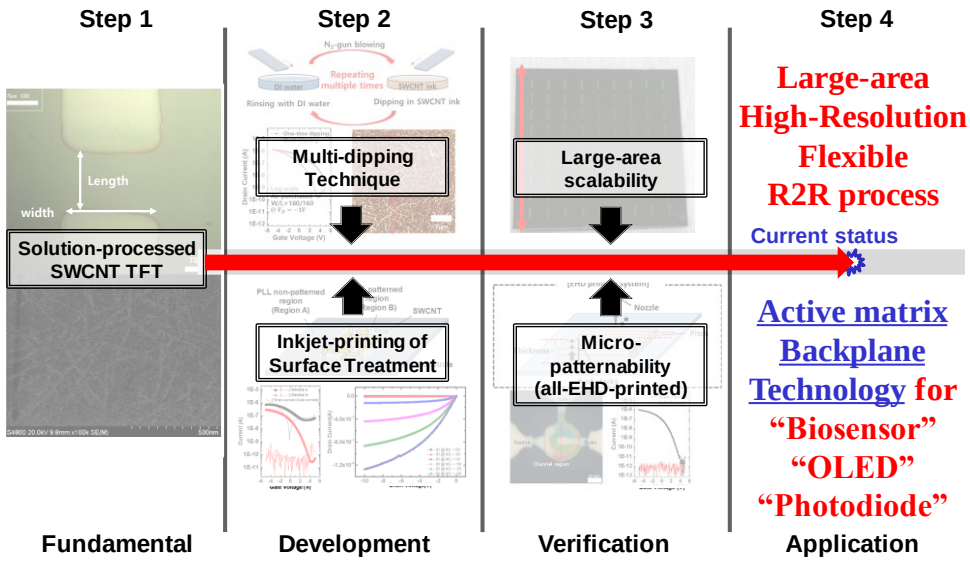

Figure 5.3. Roadmap of solution-processed SWCNT TFT based on this dissertation.

Reference

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Appendix

Certain portions of the work discussed in this dissertation are also discussed in the following publications:

[1] **H. Kim**, J. Seo, N. Seong, S. Lee, S. Lee, T. Kim*, Y. Hong*, “Multi-Dipping Technique for Fabrication Time Reduction and Performance Improvement of Solution-Processed Single-walled Carbon Nanotube Thin-Film Transistors”, *Adv. Eng. Mater.* 1901413 (2020).

[2] **H. Kim**, J. Seo, N. Seong, T. Kim, S. Lee, and Y. Hong*, "Solution-processed single-walled carbon nanotube thin film transistor In-situ patterned by inkjet-printing of surface treatment material", *SID Symposium Dig. Tech. Pap.* **50**, 1321-1324 (2019).

[3] N. Seong†, **H. Kim**†, and Y. Hong*, "All Electrohydrodynamic-jet printed Highly integrated and High-resolution Active Pixel Design with Vertically stacked Single-walled Carbon Nanotube Thin-film Transistors and in-situ Via-hole Formation Technology” (virtual title), **submission in preparation** (equally contributed).

Publication List

International Journals

1. **H. Kim**, J. Seo, N. Seong, S. Lee, S. Lee, T. Kim*, Y. Hong*, “Multi-Dipping Technique for Fabrication Time Reduction and Performance Improvement of Solution-Processed Single-walled Carbon Nanotube Thin-Film Transistors”, *Adv. Eng. Mater.* 1901413 (2020). **(Front Cover Image Paper)**
2. N. Seong†, **H. Kim**†, and Y. Hong*, "All Electrohydrodynamic-jet printed Highly integrated and High-resolution Active Pixel Design with Vertically stacked Single-walled Carbon Nanotube Thin-film Transistors and in-situ Via-hole Formation Technology" (virtual title), **submission in preparation** (equally contributed).
3. N. Seong, T. Kim, **H. Kim**, T. J. Ha*, and Y. Hong*, “Tunable threshold voltage in solution processed single-walled carbon nanotube thin film transistors”, *Curr. Appl. Phys.* **15**, S1-S8 (2015).
4. T. Kim, N. Seong, J. Ha, **H. Kim**, T. J. Ha*, and Y. Hong*, "The rapid and dense assembly of solution processed single wall carbon nanotube semiconducting films via an acid based additive in the aqueous dispersion", *J. Mater. Chem. C* **4**, 5461-5468 (2016).
5. H. Yoo, J. Ha, **H. Kim**, J. Seo, S. Lee*, Y. Hong*, “Tunable Stability of All-Inkjet-Printed Double-Gate Carbon Nanotube Thin Film Transistors”, *IEEE Electron Device Lett.* **41**, 860-863 (2020).

6. J. Seo, J. Ha, B. Lee, **H. Kim**, Y. Hong*, “Fluoroelastomer encapsulation for enhanced reliability of solution-processed carbon nanotube thin-film transistors”, *Thin Solid Films* **704**, 138021 (2020).

International/Domestic Conference

1. **H. Kim**, T. Kim, N. Seong, J. Ha, and Y. Hong*, "Inkjet-Printed Source/Drain Contact for Solution-Processed Single-Walled Carbon Nanotube Thin-Film Transistors", The 22nd Korean Conference on Semiconductors, Incheon, Korea, February (2015) (poster) **(Best Poster Award in Nano-Science & Technology Session)**
2. **김형규**, 김태훈, 성낙현, 홍용택*, “용액공정기반 단일벽탄소나노튜브 박막트랜지스터 어레이 구현 및 특성 분석”, 2015년도 대한전자공학회 추계종합학술대회, Wonju, Korea, November (2015) (oral)
3. **H. Kim**, T. Kim, J. Seo, N. Seong, and Y. Hong*, “Solution-Processed Thin Film Transistors with SWCNTs patterned by In-situ UVO Treatment”, The 27th International Conference on Amorphous and Nanocrystalline Semiconductors (ICANS 27), Seoul, Korea, August (2017) (poster)
4. **H. Kim**, J. Seo, N. Seong, T. Kim, S. Lee, and Y. Hong*, "Solution-processed single-walled carbon nanotube thin film transistor *In-situ* patterned by inkjet-printing of surface treatment material", SID Display Week 2019, San Jose, May (2019) (poster)
5. J. Ha, T. Kim, N. Seong, **H. Kim** and Y. Hong*, "In Situ Fabrication of all-inkjet-printed Carbon Nanotube Thin-Film Transistors Directly Onto Stretchable Substrate", International Conference on Electronic Materials

and Nanotechnology for Green Environment 2014 (ENGE 2014), Jeju, Korea, November (2014) (oral)

6. T. Kim, N. Seong, **H. Kim**, T.-J. Ha and Y. Hong*, "Improved Random Networks of Solution-processed Single-walled Carbon Nanotube with Reduced Deposition Time by using Nitric Acid", International Conference on Electronic Materials and Nanotechnology for Green Environment 2014 (ENGE 2014), Jeju, Korea, November (2014) (oral)
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8. 성낙현, 김태훈, 지선범, **김형규**, 홍용택*, "저온 용액공정 기반 저전압 구동 단일벽 탄소나노튜브 박막 트랜지스터", 2015년도 대한전자공학회 추계종합학술대회, Wonju, Korea, November (2015) (oral)
9. Y. Hong*, S. Ji, H. Im, Y. Hong, D. Kim, **H. Kim**, N. Seong, Y. Park, Y. Joo, T. Kim, "Low voltage solution processed IGZO TFTs for CMOS circuit applications", The 3rd International Conference on Advanced Electromaterials (ICAE 2015), Jeju, Korea, November (2015) (invited talk)
10. J. Seo, J. Ha, T. Kim, N. Seong, **H. Kim**, and Y. Hong*, "Reduced turn-on voltage of all-solution-processed single-walled carbon nanotube thin-film transistors encapsulated with PDMS elastomer", The 8th International Workshop on Flexible & Printable Electronics (IWFPE 2016), Jeonju, Korea, November (2016) (poster)

11. J. Seo, J. Ha, B. Lee, **H. Kim**, and Y. Hong*, “Hysteresis-free All-solution-processed Single-Walled Carbon Nanotube Thin-film Transistors Encapsulated with Fluoropolymer”, The 27th International Conference on Amorphous and Nanocrystalline Semiconductors (ICANS 27), Seoul, Korea, August (2017) (poster)
12. H. Yoo, J. Ha, **H. Kim**, J. Seo, and Y. Hong*, “Threshold Voltage Tuning and Power Consumption Reduction of Single-Walled Carbon Nanotube Transistors Using Double Gate Structure”, The 27th International Conference on Amorphous and Nanocrystalline Semiconductors (ICANS 27), Seoul, Korea, August (2017) (poster) (Best Poster Award)
13. H. Yoo, J. Ha, **H. Kim**, J. Seo, and Y. Hong*, “A Compensation Circuit without Time Division Using Double-Gate Structured Single-Walled Carbon Nanotube Thin Film Transistors”, The 18th International Meetings on Information Display (IMID 2018), Busan, Korea, August (2018) (poster)
14. B. Park, J. Jang, **H. Kim**, J. Seo, H. Yoo, and Y. Hong*, "Aligned Single-Walled Carbon Nanotube Thin Film Transistors by One Droplet Treatment", ITC 2019, Okinawa, February (2019) (oral)
15. B. Park, J. Jang, S. Lee, **H. Kim**, J. Seo, H. Yoo and Y. Hong*, "Large-Area Assembly of Aligned Silver Nano-wires Conductors using Parallel Half-cylinder Barrier by Solution Process", The 19th International Meeting on Information Display 2019 (IMID 2019), Gyeongju, Korea, August (2019) (Poster)
16. H. Yoo, J. Ha, **H. Kim**, J. Seo, and Y. Hong*, "Double-Gate-Structured Carbon Nanotube Thin Film Transistors", The 19th International Meeting

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Patents

1. 홍용택, 김태훈, **김형규**, "표면처리물질의 인쇄공정을 이용한 탄소나노튜브 패터닝 방법", 10-2019-0064556, 서울대학교산학협력단 (2019) (국내특허, 출원)

국 문 초 록

최근 유연 및 신축성 전자 소자 응용에 대한 수요가 증가함에 따라, 용액공정기반의 시스템을 구현하는 기반 기술들이 계속해서 발전해오고 있다. 특히, 용액공정기반으로 제작된 반도성 단일벽 탄소나노튜브의 랜덤한 네트워크는 전기적, 기계적으로 우수한 성질을 가지고 있어, 대면적 액티브 매트릭스 기반의 발광 소자 및 센서와 같은 다양하고 새로운 차세대 응용 소자의 기본이 되는 박막 트랜지스터 (TFT)의 반도체층 물질로서 널리 연구되어 왔다. 또한, 저비용, 저온 공정이 가능한 분산된 형태의 고순도 반도성 단일벽 탄소나노튜브용액은 대면적의 유연/신축성 전자 소자로의 응용을 가능하게 해주었다. 이 때, 용액 공정 기반으로 탄소나노튜브 네트워크를 형성할 수 있는 여러 방법들 중에서, 박막 트랜지스터 소자의 채널 영역을 쉽고 효율적으로 제작하기 위한 방법 중 하나는, 직접 기판을 단일벽 탄소나노튜브 용액에 담그는 “직접 담그는 방법(Direct dipping method)”의 형태이며, 이는 대면적에 단일벽 탄소나노튜브를 매우 쉽고 균일하게 형성할 수 있다. 하지만 이 방법에는 크게 두 가지의 기술적인 한계점들이 존재한다. 우선, 수용액 형태의 용액을 사용하게 되면 매우 긴 공정 시간으로 인해 그 수율이 매우 낮아지게 되며, 다른 하나는 기판 전체가 용액으로 들어가기 때문에 이로부터 추가적인 패터닝 과정이 필요로 한다는 점이다. 따라서, 이 문제점들을 해결하기 위하여, 본인은 다양한 공학적인 접근 방법들을 시도해보았다.

본 학위 논문에서는, 위에서 언급된 “직접 담그는 방법”의 문제점들을 해결하기 위한 새로운 쉽고 효과적인 기반 기술들을 개발하였다. 첫 번째 기술 (multi-dipping technique, 반복적 담금기법)은 기판을 용액에 오랜 시간 담가 두는 이전의 방법과는 달리, 기판을 탄소나노튜브 용액 안에 짧은 시간 동안만 담그고 이를 탈 이온수를 이용하여 세정한 뒤, 앞에서 언급한 공정을 계속해서 반복하여 준다. 이는 기존의 “직접 담그는 방법”과는 달리 단일벽 탄소나노튜브 기반의 박막 트랜지스터의 공정 시간을 절반 이상 감소시켜줄 뿐 아니라, 그 전기적인 특성 또한 향상시켜준다. 또한, 두 번째 기술 (self-patterning technology, 표면처리물질 인쇄공정기법)은, 반도성 단일벽 탄소나노튜브와 기판 사이의 접착력을 좋게 해주는 표면처리물질을 채널을 형성하고자 하는 부분에만 잉크젯프린팅을 해주어 원하는 패턴을 형성한다. 특히 본 논문에서는 표면처리물질로서 poly-L-lysine (PLL)을 이용하였다. 이 기술을 이용할 경우, 기판 전체를 탄소나노튜브 용액에 담금에도 불구하고 반도성 단일벽 탄소나노튜브 네트워크는 오로지 추가적인 패터닝과정 없이도 공정 과정 내에서 스스로 표면처리물질 (PLL)이 인쇄된 부분에만 형성됨을 확인할 수 있었다.

또한, 단일벽 탄소나노튜브 기반의 박막 트랜지스터를 보다 효율적으로 형성해주기 위하여 두 기술을 결합하여 새로운 하나의 기술로 정의 (fast and self-patterning technique)한 후, 해당 기술이 높은 수율 및 해상도를 가지는 단일벽 탄소나노튜브 기반 박막 트랜지스터를 형성할 수 있을지에 대한 실현 및 적용 가능성을 검증하였다. 검증과정에

서는, 대면적 소자 제작에 적용 가능할 수 있는지에 대한 부분과 미세화된 소자 제작에 적용 가능한지에 대한 부분, 총 두 가지 기준점을 가지고 연구를 진행하였으며, 이 중에서 미세 패턴 가능성을 보기 위해서는 미세 패턴을 효율적으로 형성할 수 있는 전기수력학방식의 프린팅 기법(EHD printing)을 활용하였다.

본 학위논문은 다양한 기판에서 원하는 위치에 효과적으로 고품질의 단일벽 탄소나노튜브를 붙여줄 수 있는 기술들을 개발하고, 그 기술들을 결합하여 미래의 전자 소자 제작에 적합한지에 대한 적용가능성을 평가해 보는 것을 주 목적으로 하였다. 또한, 단일벽 탄소나노튜브 물질의 저온 공정 가능성과 물질 자체가 가지고 있는 우수한 기계적 특성은 본인이 개발한 기술과 함께, 가까운 미래에 차세대 유연/신축성 소자를 위한 높은 수율, 높은 해상도, 높은 성능을 가지는 단일벽 탄소나노튜브 어레이를 롤투롤 방식의 공정 기법으로 형성하는 것에 대한 지침을 제공해줄 수 있으며, 결과적으로 차세대 유연 응용 전자 소자 구현에 큰 기여를 할 수 있을 것으로 기대된다.

키워드 : 용액공정; 반도성 단일벽 탄소나노튜브; 반복적 담금기법; 표면처리물질 인쇄공정기법; 대면적 적용가능성; 미세 패턴 가능성

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Effective Solution-processed Deposition Techniques of Semiconducting Single-walled Carbon Nanotube for Next-generation Thin-Film Transistor

차세대 박막 트랜지스터를 위한 효율적인 용액공정기반 반도성 단일벽 탄소나노튜브의 박막 형성 방법들에 관한 연구

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